

PHOTORESIST DESIGN LAYOUT PATTERN PROXIMITY CORRECTION THROUGH FAST EDGE PLACEMENT ERROR PREDICTION VIA A PHYSICS- BASED ETCH PROFILE MODELING FRAMEWORK

ABSTRACT

Disclosed are methods of generating a proximity-corrected design layout for photoresist to be used in an etch operation. The methods may include identifying a feature in an initial design layout, and estimating one or more quantities characteristic of an in-feature plasma flux (IFPF) within the feature during the etch operation. The methods may further include estimating a quantity characteristic of an edge placement error (EPE) of the feature by comparing the one or more quantities characteristic of the IFPF to those in a look-up table (LUT, and/or through application of a multivariate model trained on the LUT, e.g., constructed through machine learning methods (MLM)) which associates values of the quantity characteristic of EPE with values of the one or more quantities characteristics of the IFPF. Thereafter, the initial design layout may be modified based on at the determined quantity characteristic of EPE.

Fig. 11B