

Description

Technical Field

This invention relates generally to gate arrays, and, more particularly, to power bus routing for gate arrays.

Background Art

Gate arrays are uniform patterns of hundreds or thousands of unconnected transistor-level gate cells. Due to the availability to a designer of means to connect the cells via interlevel contacts and interlevel routing performed at a late stage in processing, many custom circuits may be created from a basic gate array. A basic design objective of gate arrays is to make the gate cells easily accessible to power and ground busses since the gate cells are typically placed on a level different from the power and ground busses.

From United States Patent No. 4412237 there is known a gate array comprising columns of a plurality of transistor cells, where n is an integer, each of said n columns of transistor cells having first and second power busses coupled to first and second voltage potential lines, respectively, and extending substantially along each of the columns. However, when hundreds or thousands of transistors are connected in an array, very large current spikes may develop in certain locations of the array when the transistors switch at the same time. When power busses are not routed closely to the transistors, noise may exist on internal nodes and create logic errors in the gate array cells. When current spikes exist at the inputs of the gate array, these spikes may also create logic errors in the internal portion of the gate array. Some gate arrays utilize separate digital and analog power and ground distribution busses to minimize analog circuit noise from digital circuitry as noted on page 166 of "CMOS Uncommitted Logic Arrays Are Part-Digital, Part-Analog", by Yoder, *Electronics*, January 13, 1981.

However, when such gate arrays have a large plurality of input/output cells per side of the array, large current spikes at the output may still generate noise errors in the internal digital circuitry.

Brief Summary of the Invention

It is an object of the present invention to provide a gate array wherein the above disadvantages may be overcome.

In accordance with the present invention as claimed there are provided a gate array and a method of isolating noise from an external source in a gate array characterized in that the gate array further comprises: a power strip extending substantially perpendicular to said n columns and coupling said first and second power busses of a plurality of the columns to said first and second voltage potential lines, respectively, for providing increased current capability to said plurality of transistor cells; a plurality of output cells along one or more sides of the gate array; and output power busses positioned along the outer perimeter of said gate array for providing power busses

for the output cells which are separate from the first and second voltage potential lines used to provide power to the transistor cells, said output power busses keeping external current spikes from being coupled into the array. The above and other features and advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawing.

Brief Description of the Drawing

The single Figure illustrates in graphic form a gate array constructed in accordance with a preferred embodiment of the present invention.

Description of a Preferred Embodiment

Shown in the single drawing is a gate array 10 having n columns of transistor cells, such as column 12 having cells 14 and 16, where n is an integer. Although in a preferred form eighteen columns of transistor cells are shown, any number of columns and cells may be used to practise the invention. If gate array 10 is viewed from the left or right side of the drawing, the columns can be considered as rows. Extending the entire length of each of the n columns are first and second power busses, such as power bus 18 and power bus 20 in column 12. The first and second busses in the n columns are coupled to a first and a second voltage potential line, respectively, by coupling each power bus to either an input/internal logic power bus 22 or an input/internal logic power bus 24. It should be noted that not all gate arrays have a plurality of continuous columns of transistor cells, but rather may have columns of cells divided into two or more sections. For gate arrays having sectioned columns of transistor cells, power busses, such as power busses 18 and 20 may not extend the entire length of each column across the plural sections. However, this invention may be practised for gate arrays having any variety of structural organization of transistor cells. In a preferred form, input/internal logic power bus 22 is at a V_{ss} potential and extends substantially around the perimeter of the n columns. Input/internal logic power bus 24 is at a V_{DD} potential and also extends substantially around the perimeter of the n columns in a preferred form. Conventionally, the V_{DD} potential is a positive voltage potential and the V_{ss} potential is more negative than V_{DD} although V_{DD} is not necessarily a positive voltage potential. Although input/internal logic power busses 22 and 24 encircle the n columns for noise reduction purposes, the input/internal logic power busses need only to be long enough to be physically connected to each pair of power busses of the n columns. On the outer sides of a first column 26 and an n th column 28 are output power busses 30 and 32, respectively, which are coupled to voltage potential V_{DD} . Extending around the outside perimeter of gate array 10 is an output power bus 34 which is coupled to V_{ss} potential. The output power busses are so designated because they primarily supply power to output circuits. Output power

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busses 30 and 34 form a first pair of output busses which, in a preferred form, extend substantially parallel to and along the outside edge of first column 26. Similarly, output power busses 32 and 34 form a second pair of output busses which extend substantially parallel to and along the outside edge of nth column 28 in a preferred form. In yet another form of the invention, output power busses 30 and 32 may be extended in part, or substantially around the perimeter of the n columns. Further, output power busses 30 and 32 may extend substantially parallel to output power bus 34 and be connected to function as a single power output power bus. Power strips 36, 38 and 40 extend substantially perpendicular to the n columns and are coupled to busses 22 and 24 at each end at the outside edge of columns 26 and 28. Power strips 36, 38 and 40 each comprise first and second conductive busses, the first of which is connected to input/internal logic power bus 22 at the outside edge of columns 26 and 28. The second conductive bus of power strips 36, 38 and 40 is connected to input/internal logic power bus 24 at the outside edge of columns 26 and 28. In the preferred form, the power busses in the n columns, such as power busses 18 and 20, are routed on a first layer of metal which is covered by an insulating dielectric layer. Power strips 36, 38 and 40 are routed on a second layer of metal so that power strips 36, 38 and 40 do not electrically short circuit the transistor cells of the n columns. The conductive busses of strips 36, 38 and 40 which are connected to input/internal logic power bus 22 are also connected to the first power bus of each column, such as power bus 18 in column 12. This connection is made by cutting a hole, or a via, through the dielectric separating the n columns from power strips 36, 38 and 40. The conductive busses of strips 36, 38 and 40 which are connected to internal logic power bus 24 are connected to the second power bus of each column, such as power bus 20 in column 12. In the preferred form, three power strips are utilized and the first and second conductive bus of power strip 38 is made twice as large as the conductive busses of power strips 36 and 40. However, the invention may be practised with one or any plurality of power strips. It should also be noted that power strips 36, 38 and 40 need not necessarily extend across all the columns or gate array 10. Current availability may be increased by using some or all power strips across only a portion of the n columns.

In operation, a gate array, regardless of what type of process is used to manufacture the array, will usually develop very large current spikes when the transistors in the transistor cells switch. An entire column of transistors may switch at the same time and generate current in the hundreds of milliamperes range. Such current spikes can change the internal logic circuitry and create erroneous data. Conventional power bus routing is not sufficient to keep voltage drops in the cells associated with the current spikes from becoming excessive. Furthermore, in gate arrays there are typically a large number of output cells such as

output cell 42 on one or more sides of the gate array with each cell having a contact pad. With a large number of output cells existing, the possibility for large AC and DC loads to be applied thereto exists. Therefore to keep current spikes from entering the array matrix, power busses, such as busses 30, 32 and 34, which are separate from the power busses of the internal logic circuitry and input pads, such as busses 22 and 24, are used for the output circuits.

To substantially reduce the size of current spikes in each column, the effective ohmic length of the power busses of the n columns is reduced by adding power strips 36, 38 and 40 and connecting them to the power busses of the n columns. If power strips 36, 38 and 40 are routed on a different layer of metal and separated from the power busses of the n columns by a dielectric layer, the logic routing of a conventional gate array has not been disrupted. By now it should be appreciated that a gate array having power routing which separates current spikes in the output cells from internal digital logic and input pins and which minimizes current spikes in the digital logic has been provided.

By having input/internal logic power busses which are separate from output power busses, noise external to gate array 10 is effectively isolated. Furthermore, when separate power busses are used in this manner, the busses may be coupled to different leads in an integrated circuit package and different voltage levels applied thereto.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the scope of the invention, as defined by the appended claims.

Claims

1. A gate array (10) comprising:

n columns (26, 28) of a plurality of transistor cells (14, 16), where n is an integer, each of said n columns (26, 28) of transistor cells (14, 16) having first and second power busses (18, 20) coupled to first and second voltage potential lines (22, 24), respectively, and extending substantially along each of the columns (26—28),

characterized in that the gate array further comprises:

a power strip (36) extending substantially perpendicular to said n columns (26, 28), and coupling said first and second power busses (18, 20) of a plurality of the columns to said first and second voltage potential lines (22, 24), respectively, for providing increased current capability to said plurality of transistor cells (14, 16);

a plurality of output cells (42) along one or more sides of the gate array (10); and

busses 30 and 34 form a first pair of output busses which, in a preferred form, extend substantially parallel to and along the outside edge of first column 26. Similarly, output power busses 32 and 34 form a second pair of output busses which extend substantially parallel to and along the outside edge of nth column 28 in a preferred form. In yet another form of the invention, output power busses 30 and 32 may be extended in part, or substantially around the perimeter of the n columns. Further, output power busses 30 and 32 may extend substantially parallel to output power bus 34 and be connected to function as a single power output power bus. Power strips 36, 38 and 40 extend substantially perpendicular to the n columns and are coupled to busses 22 and 24 at each end at the outside edge of columns 26 and 28. Power strips 36, 38 and 40 each comprise first and second conductive busses, the first of which is connected to input/internal logic power bus 22 at the outside edge of columns 26 and 28. The second conductive bus of power strips 36, 38 and 40 is connected to input/internal logic power bus 24 at the outside edge of columns 26 and 28. In the preferred form, the power busses in the n columns, such as power busses 18 and 20, are routed on a first layer of metal which is covered by an insulating dielectric layer. Power strips 36, 38 and 40 are routed on a second layer of metal so that power strips 36, 38 and 40 do not electrically short circuit the transistor cells of the n columns. The conductive busses of strips 36, 38 and 40 which are connected to input/internal logic power bus 22 are also connected to the first power bus of each column, such as power bus 18 in column 12. This connection is made by cutting a hole, or a via, through the dielectric separating the n columns from power strips 36, 38 and 40. The conductive busses of strips 36, 38 and 40 which are connected to internal logic power bus 24 are connected to the second power bus of each column, such as power bus 20 in column 12. In the preferred form, three power strips are utilized and the first and second conductive bus of power strip 38 is made twice as large as the conductive busses of power strips 36 and 40. However, the invention may be practised with one or any plurality of power strips. It should also be noted that power strips 36, 38 and 40 need not necessarily extend across all the columns or gate array 10. Current availability may be increased by using some or all power strips across only a portion of the n columns.

In operation, a gate array, regardless of what type of process is used to manufacture the array, will usually develop very large current spikes when the transistors in the transistor cells switch. An entire column of transistors may switch at the same time and generate current in the hundreds of milliamperes range. Such current spikes can change the internal logic circuitry and create erroneous data. Conventional power bus routing is not sufficient to keep voltage drops in the cells associated with the current spikes from becoming excessive. Furthermore, in gate arrays there are typically a large number of output cells such as

output cell 42 on one or more sides of the gate array with each cell having a contact pad. With a large number of output cells existing, the possibility for large AC and DC loads to be applied thereto exists. Therefore to keep current spikes from entering the array matrix, power busses, such as busses 30, 32 and 34, which are separate from the power busses of the internal logic circuitry and input pads, such as busses 22 and 24, are used for the output circuits.

To substantially reduce the size of current spikes in each column, the effective ohmic length of the power busses of the n columns is reduced by adding power strips 36, 38 and 40 and connecting them to the power busses of the n columns. If power strips 36, 38 and 40 are routed on a different layer of metal and separated from the power busses of the n columns by a dielectric layer, the logic routing of a conventional gate array has not been disrupted. By now it should be appreciated that a gate array having power routing which separates current spikes in the output cells from internal digital logic and input pins and which minimizes current spikes in the digital logic has been provided.

By having input/internal logic power busses which are separate from output power busses, noise external to gate array 10 is effectively isolated. Furthermore, when separate power busses are used in this manner, the busses may be coupled to different leads in an integrated circuit package and different voltage levels applied thereto.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the scope of the invention, as defined by the appended claims.

Claims

1. A gate array (10) comprising:

n columns (26, 28) of a plurality of transistor cells (14, 16), where n is an integer, each of said n columns (26, 28) of transistor cells (14, 16) having first and second power busses (18, 20) coupled to first and second voltage potential lines (22, 24), respectively, and extending substantially along each of the columns (26—28),

characterized in that the gate array further comprises:

a power strip (36) extending substantially perpendicular to said n columns (26, 28), and coupling said first and second power busses (18, 20) of a plurality of the columns to said first and second voltage potential lines (22, 24), respectively, for providing increased current capability to said plurality of transistor cells (14, 16);

a plurality of output cells (42) along one or more sides of the gate array (10); and



Output power busses (30, 32) positioned along the outer perimeter of said gate array (10), for providing power busses for the output cells (42) which are separate from the first and second voltage potential lines (22, 24) used to provide power to the transistor cells (14, 16), said output power busses keeping external current spikes from being coupled into the array (10).

2. A gate array (10) according to claim 1 comprising:

three power strips (36, 38, 40) extending substantially perpendicular to said n columns (26, 28) from the first to the n th column and spaced a substantially equal distance apart, said second power strip (38) located between said first (36) and third (40) power strips, wherein the width of said second power strip (38) is substantially larger than the width of said first (36) and third (40) power strips.

3. A gate array (10) according to claim 1, wherein the output power busses (30, 32) further comprise:

a first output power bus (34) positioned completely around the perimeter of the gate array (10); and

second (30) and third (32) output power busses positioned parallel to and between the first output power bus (34) and said first (26) and n th (28) columns, respectively, wherein the first output power bus (34) provides a first voltage potential and said second (30) and third (32) output power busses each provide a second voltage potential.

4. A gate array (10) according to claim 1 wherein said first and second power busses (18, 20) of each of said n columns are routed on a first conductive layer and said power strip (36) is routed on a second conductive layer which is separated from said first conductive layer by a dielectric layer.

5. A gate array (10) according to claim 1 further comprising:

second (38) and third (40) power strips extending substantially perpendicular to said n columns and spaced apart to divide said gate array (10) into four sections.

6. A method of isolating noise from an external source in a gate array (10) having a plurality of transistor cells (14, 16) arranged in n columns (26, 28), where n is an integer, substantially each column having first and second power busses (18, 20) coupled to first and second voltage potential lines (22, 24) respectively, and extending substantially along each of the columns (26, 28),

characterized by:

providing a power strip (36) extending substantially perpendicular to said n columns (26, 28) which couples the first and second power busses (18, 20) of a plurality of the columns to the first and second voltage potential lines (22, 24) for providing increased current capability to the plurality of transistor cells (14, 16);

providing a plurality of output cells (42) along one or more sides of the gate array (10); and

providing power busses (30, 32) along the outer perimeter of the gate array (10) for the output

cells (42), said power busses being separated from the first and second voltage potential lines (22, 24) used to provide power to the transistor cells (14, 16), thereby keeping external current spikes from being coupled into the array (10).

Patentansprüche

1. Gategruppe (10), enthaltend:

n Spalten (26, 28) einer Mehrzahl von Transistorzellen (14, 16), wobei n eine ganze Zahl ist, jede der n Spalten (26, 28) aus Transistorzellen (14, 16) erste und zweite Stromversorgungsleitungen (18, 20) haben, die mit ersten bzw. zweiten Spannungspotentialleitungen (22, 24) verbunden sind und sich im wesentlichen längs einer jeden der Spalten (26, 28) erstrecken,

dadurch gekennzeichnet, daß die Gate-Gruppe weiterhin enthält:

einen Stromversorgungstreifen (36), der sich im wesentlichen senkrecht zu den n Spalten (26, 28) erstreckt und die ersten und zweiten Stromversorgungsleitungen (18, 20) einer Mehrzahl der Spalten mit den ersten bzw. zweiten Spannungspotentialleitungen (22, 24) verbindet, um ein gesteigertes Stromleitvermögen zu der Vielzahl Transistorzellen (14, 16) zu erzeugen;

eine Vielzahl von Ausgangszellen (42) längs einer oder mehrerer Seiten der Gate-Gruppe (10); und

Ausgangsstromversorgungsleitungen (30, 32), die längs des äußeren Umfangs der Gate-Gruppe (10) angeordnet sind, um Stromversorgungsleitungen für die Ausgangszellen (42) zu bilden, die getrennt von den ersten und zweiten Spannungspotentialleitungen (22, 24), die für die Stromversorgung der Transistorzellen (14, 16) verwendet werden, getrennt sind, wobei die Ausgangsstromversorgungsleitungen externe Stromspitzen daran hindern, in die Gruppe (10) eingekoppelt zu werden.

2. Gate-Gruppe (10) nach Anspruch 1, enthaltend

drei Stromversorgungstreifen (30, 38, 40), die sich im wesentlichen senkrecht zu den n Spalten (26, 28) von der ersten zur n -ten Spalte erstrecken und im wesentlichen gleichen Abstand haben, wobei der zweite Stromversorgungstreifen (38) zwischen dem ersten (36) und dem dritten (40) Stromversorgungstreifen angeordnet ist, wobei die Breite des zweiten Stromversorgungstreifens (38) wesentlich größer als die Breite der ersten (36) und dritten (40) Stromversorgungstreifen ist.

3. Gate-Gruppe (10) nach Anspruch 1, bei der die Ausgangsstromversorgungsleitungen (30, 32) weiterhin enthalten:

eine erste Ausgangsstromversorgungsleitung (34), die vollständig um den Umfang der Gate-Gruppe (10) angeordnet ist; und

zweite (30) und dritte (32) Ausgangsstromversorgungsleitungen, die parallel zu und zwischen der ersten Ausgangsstromversorgungsleitung (34) und den ersten (26) bzw. n -ten (28) Spalten angeordnet sind, wobei die erste Ausgangsstrom-



Versorgungsleitung (34) ein erstes Spannungspotential anbietet und die zweiten (30) und dritten (32) Ausgangsstromversorgungsleitungen jeweils ein zweites Spannungspotential anbieten.

4. Gate-Gruppe (10) nach Anspruch 1, bei der die ersten und zweiten Stromversorgungsleitungen (18, 20) einer jeden der n Spalten auf einer ersten leitfähigen Schicht verlegt sind und der Stromversorgungstreifen (36) auf einer zweiten leitfähigen Schicht verlegt ist, die von der ersten leitfähigen Schicht durch eine dielektrische Schicht getrennt ist.

5. Gate-Gruppe (10) nach Anspruch 1, weiterhin enthaltend:

zweite (38) und dritte (40) Stromversorgungstreifen, die sich im wesentlichen senkrecht zu den n Spalten erstrecken und voneinander Abstand haben, um die Gate-Gruppe (10) in vier Sektionen zu teilen.

6. Verfahren zum Isolieren von von einer externen Quelle stammenden Strömungen von einer Gate-Gruppe (10), die eine Vielzahl von Transistorzellen (14, 16) aufweist, die in n Spalten (26, 28) angeordnet sind, wobei n eine ganze Zahl ist, im wesentlichen jede Spalte erste und zweite Stromversorgungsleitungen (18, 20) hat, die mit ersten bzw. zweiten Spannungspotentialleitungen (22, 24) verbunden sind und sich im wesentlichen längs der Spalten (26, 28) erstrecken, gekennzeichnet durch:

Bereitstellen eines Stromversorgungstreifens (36), der sich im wesentlichen senkrecht zu den n Spalten (26, 28) erstreckt, der die ersten und zweiten Stromversorgungsleitungen (18, 20) einer Vielzahl der Spalten mit ersten und zweiten Spannungspotentialleitungen (22, 24) verbindet, um ein gesteigertes Stromleitvermögen zu der Vielzahl der Transistorzellen (14, 16) zu erzeugen;

Erstellen einer Vielzahl von Ausgangszellen (42) längs einer oder mehrerer Seiten der Gate-Gruppe (10) und

Anordnen von Stromversorgungsleitungen (30, 32) längs des äußeren Umfangs der Gate-Gruppe (10) für die Ausgangszellen (42), wobei die Stromversorgungsleitungen von den ersten und zweiten Spannungspotentialleitungen (22, 24) getrennt sind, die dazu verwendet werden, Strom zu den Transistorzellen (14, 16) zu führen, um dadurch äußere Stromspitzen davon abzuhalten, in die Gruppe (10) eingekoppelt zu werden.

Revendications

1. Réseau de portes (10) comprenant:

n colonnes (26, 28) d'un ensemble de cellules à transistor (14, 16), n étant un entier, chacune des n colonnes (26, 28) des cellules à transistor (14, 16) comportant des premier et deuxième bus d'alimentation (18, 20) couplés respectivement à des première et deuxième lignes de potentiel de tension (22, 24), et s'étendant essentiellement le long de chacune des colonnes (26—28),

caractérisé en ce que le réseau de portes comprend en outre:

une bande d'alimentation (36) s'étendant

essentiellement perpendiculairement aux n colonnes (26, 28), et reliant les premier et deuxième bus d'alimentation (18, 20) d'un ensemble des colonnes aux première et deuxième lignes de potentiel de tension (22, 24), respectivement, pour fournir une capacité de courant accrue à l'ensemble des cellules à transistor (14, 16);

un ensemble de cellules de sortie (42) le long d'un ou de plusieurs côtés du réseau de portes (10); et

des bus d'alimentation de sortie (30, 32) placés le long du périmètre extérieur du réseau de portes (10), pour fournir des bus d'alimentation pour les cellules de sortie (42) qui sont séparés des première et deuxième lignes de potentiel de tension (22, 24) utilisées pour fournir une alimentation aux cellules à transistor (14, 16), les bus d'alimentation de sortie empêchant que des pointes de courant extérieures soient envoyées dans le réseau (10).

2. Réseau de portes (10) selon la revendication 1, comprenant:

trois bandes d'alimentation (36, 38, 40) s'étendant essentiellement perpendiculairement aux n colonnes (26, 28) de la première à la n^{ème} colonne et espacées d'une distance essentiellement égale, la deuxième bande d'alimentation (38) placée entre la première (36) et la troisième (40) bande d'alimentation et la largeur de cette deuxième bande d'alimentation (38) étant essentiellement supérieure à la largeur des première (36) et troisième (40) bandes d'alimentation.

3. Réseau de portes (10) selon la revendication 1, dans lequel les bus d'alimentation de sortie (30, 32) comprennent en outre:

un premier bus d'alimentation de sortie (34) placé complètement autour du périmètre du réseau de portes (10); et

des deuxième (30) et troisième (32) bus d'alimentation de sortie placés parallèlement à et entre le premier bus d'alimentation de sortie (34) et les première (26) et n^{ème} (28) colonnes, respectivement, où le premier bus d'alimentation de sortie (34) fournit un premier potentiel de tension et les deuxième (30) et troisième (32) bus d'alimentation de sortie fournissent chacun un deuxième potentiel de tension.

4. Réseau de portes (10) selon la revendication 1, dans lequel les premier et deuxième bus d'alimentation (18, 20) de chacune des n colonnes sont acheminés sur une première couche conductrice et la bande d'alimentation (36) est acheminée sur une deuxième couche conductrice qui est séparée de la première couche conductrice par une couche diélectrique.

5. Réseau de portes (10) selon la revendication 1, comprenant en outre:

des deuxième (38) et troisième (40) bandes d'alimentation s'étendant essentiellement perpendiculairement aux n colonnes et espacées pour diviser le réseau de portes (10) en quatre sections.

6. Procédé pour isoler le bruit d'une source extérieure dans un réseau de portes (10) comportant un ensemble de cellules à transistor (14, 16)



disposées en n colonnes (26, 28), n étant un entier, chaque colonne comportant essentiellement des premier et deuxième bus d'alimentation (18, 20) couplés respectivement à des première et deuxième lignes de potentiel de tension (22, 24), et s'étendant essentiellement le long de chacune des colonnes (26, 28),

caractérisé en ce qu'il consiste à:

prévoir une bande d'alimentation (36) s'étendant essentiellement perpendiculairement aux n colonnes (26, 28) qui relie les premier et deuxième bus d'alimentation (18, 20) d'un ensemble des colonnes aux première et deuxième lignes de potentiel de tension (22, 24) pour fournir une

capacité de courant accrue à l'ensemble des cellules à transistor (14, 16);

prévoir un ensemble de cellules de sortie (42) le long d'un ou de plusieurs côtés du réseau de portes (10); et

prévoir des bus d'alimentation (30, 32) le long du périmètre extérieur du réseau de portes (10) pour les cellules de sortie (42), les bus d'alimentation étant séparés des première et deuxième lignes de potentiel de tension (22, 24) utilisées pour fournir une alimentation aux cellules à transistor (14, 16), en empêchant ainsi que des pointes de courant extérieures soient envoyées dans le réseau (10).

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