

What Is Claimed Is:

1. A semiconductor device comprising:

first gate electrodes including a first lower electrode, a first upper electrode disposed above the first lower electrode and including a first pad region, and one or more first intermediate electrodes disposed between the first lower electrode and the first upper electrode; and

second gate electrodes including a second lower electrode, a second upper electrode disposed above the second lower electrode and including a second pad region, and one or more second intermediate electrodes disposed between the second lower electrode and the second upper electrode,

wherein the second gate electrodes are sequentially stacked above the first upper electrode, while exposing the first pad region along a direction orthogonal to an upper surface of the first upper electrode,

wherein the first lower electrode includes a first extending portion extending by a first length, further than the first upper electrode, in a first direction,

wherein the second lower electrode includes a second extending portion extending by a second length, further than the second upper electrode, in the first direction, and

wherein a length in the first direction of each of the first and second pad regions is greater than each of the first and second lengths of the first and second extending portions, and

wherein the second pad region, the second extending portion, the first pad region and the first extending portion are sequentially arranged in the first direction.

2. The semiconductor device of claim 1, further comprising:

a substrate; and

a lower gate electrode, comprising a lower pad region, the lower gate electrode positioned above an upper surface of the substrate,

wherein the first gate electrodes are disposed on the lower gate electrode.

3. The semiconductor device of claim 1, wherein the second length is different from the first length.

4. The semiconductor device of claim 1, wherein the second length is greater than the first length.

5. The semiconductor device of claim 1, wherein the one or more first intermediate electrodes extend by a length shorter than the first length, further than the first upper electrode, in the first direction, and

the one or more second intermediate electrodes extend by a length shorter than the second length, further than the second upper electrode, in the first direction.

6. The semiconductor device of claim 1, further comprising third gate electrodes sequentially stacked above the second upper electrode,

wherein the second upper electrode comprises a second pad region,

the third gate electrodes expose the second pad region along the direction orthogonal to the upper surface of the first upper electrode,

the third gate electrodes include a third lower electrode, a third upper electrode disposed above the third lower electrode, and one or more third intermediate electrodes disposed between the third lower electrode and the third upper electrode,

the second length is greater than the first length, and

the third lower electrode extends by a third length greater than the second length, further than the third upper electrode, in the first direction.

7. The semiconductor device of claim 1, further comprising vertical cell structures penetrating through the first and second gate electrodes,

wherein the vertical cell structures include a channel semiconductor layer spaced apart from the first and second gate electrodes, and a gate dielectric between the channel semiconductor layer and the first and second gate electrodes.

8. A semiconductor device comprising:
a substrate including a memory cell region and a contact region; and
gate electrodes disposed on the memory cell region of the substrate and extending into the contact region,

wherein the gate electrodes include word lines having word line pad regions,
the word line pad regions are arranged to have a first step in a first direction from the memory cell region to the contact region while being substantially parallel to an upper surface of the substrate, and are arranged to have a second step, smaller than the first step, in a second direction, perpendicular to the first direction, while being parallel to the upper surface of the substrate,

among the word lines, word lines located at different heights extend to have different lengths in the first direction from the memory cell region, and

wherein the word line pad regions comprise a first pad region and a second pad region,
wherein the word lines include:

a first upper word line including the first pad region;
a second lower word line disposed on the first upper word line and exposing the first pad region along a direction orthogonal to an upper surface of the first upper word line; and
a second upper word line disposed on the second lower word line and having the second pad region, and

wherein the second lower word line extends by a length shorter than a length of each of the word line pad regions, further than the second upper word line, in the first direction.

9. The semiconductor device of claim 8, further comprising vertical cell structures disposed on the memory cell region and penetrating through the gate electrodes, wherein each of the vertical cell structures includes a channel semiconductor layer.

10. The semiconductor device of claim 8, further comprising dummy vertical structures disposed on the contact region and penetrating through the gate electrodes.

11. The semiconductor device of claim 8, further comprising a first lower word line disposed under the first upper word line,

wherein the first lower word line includes a first extending portion extending by a first length, further than the first upper word line, in the first direction,

wherein the second lower word line includes a second extending portion extending by a second length, further than the second upper word line, in the first direction,

wherein the length in the first direction of each of the word line pad regions is greater than each of the first and second lengths of the first and second extending portions, and

wherein the second pad region, the second extending portion, the first pad region and the first extending portion are sequentially arranged in the first direction.

12. The semiconductor device of claim 8, further comprising:

a first contact plug on the first pad region; and

a second contact plug on the second pad region,

wherein a width of each of the first and the second contact plugs is greater than each of the first and second lengths of the first and second extending portions.

13. The semiconductor device of claim 8, wherein the gate electrodes further comprise upper gate lines disposed on the word lines and having upper pad regions,

wherein the upper gate lines include upper pad regions arranged to have a third step,

smaller than the first step in the first direction and arranged to have the same height in the second direction.

14. The semiconductor device of claim 13, further comprising:
main source structures disposed on the memory cell region and extending from the memory cell region in the first direction to transverse the contact region; and
a first secondary source structure and a second secondary source structure disposed between the main source structures and having opposing ends,
wherein the opposing ends of the first and second secondary source structures are located in the contact region.

15. The semiconductor device of claim 14, wherein the opposing ends of the first and second secondary source structures are located between the upper pad regions and the word line pad regions.

16. A semiconductor device comprising:
a first gate group including first gate electrodes extending in a first direction and sequentially stacked;
a second gate group disposed on the first gate group, and including second gate electrodes extending in the first direction and sequentially stacked, and
a first contact plug and a second contact plug sequentially arranged in the first direction,
wherein the first gate electrodes include a first lower electrode and a first upper electrode above the first lower electrode and including a first pad region,
wherein the second gate electrodes include a second lower electrode and a second upper electrode above the second lower electrode and including a second pad region,
wherein the first lower electrode includes a first extending portion extending by a first length, further than the first upper electrode, in the first direction,

wherein the second lower electrode includes a second extending portion extending by a second length, further than the second upper electrode, in the first direction,

wherein the second lower electrode exposes the first pad region along a direction orthogonal to an upper surface of the first upper electrode,

wherein a length in the first direction of each of the first and second pad regions is greater than each of the first and the second lengths of the first and second extending portions,

wherein the first contact plug is disposed on and in contact with the first pad region, and

wherein the second contact plug is disposed on and in contact with the second pad region, and

wherein a width in the first direction of each of the first and second contact plugs is greater than each of the first and the second lengths of the first and second extending portions.

17. The semiconductor device of claim 16, wherein the second length is greater than the first length.

18. The semiconductor device of claim 16, further comprising:
a channel semiconductor layer penetrating through the first and second gate electrodes;
and

a data storage layer between the first and second gate electrodes and the channel semiconductor layer.

19. The semiconductor device of claim 16, wherein the first pad region has a thickness greater than a thickness of the first upper electrode.

20. The semiconductor device of claim 16, wherein the second pad region, the

second extending portion, the first pad region and the first extending portion are sequentially arranged in the first direction.