DESCRIPTION

MONOTONIC DYNAMIC-STATIC PSEUDO-NMOS LOGIC CIRCUIT AND METHOD OF FORMING A LOGIC GATE ARRAY

Technical Field

The invention relates to CMOS gate arrays. The invention also relates to vertical ultrathin body transistors. The invention further relates to monotonic dynamic-static pseudo-NMOS logic circuits.

Background Art

CMOS technology is used for digital integrated circuits due to low power dissipation, high density of integration, and low cost of fabrication. CMOS technology is also used for analog integrated circuits.

Applications that use microelectronic components, such as telecommunications equipment, industrial control equipment, automotive electronics, etc., require more and more specialized integrated circuits. The continuing development in semiconductors has led to use of gate arrays and standard cells as a modern and inexpensive way to produce Application Specific Integrated Circuits (ASICs). An ASIC is an integrated circuit that can place on a single chip an entire system or a great part of it, performing not only digital, but also analog functions.

Gate arrays are used in ASIC design. A CMOS gate array can be described as a matrix of premanufactured (e.g., identical) cells that only requires the addition of the final metal and contact masks to define a new circuit function. Gate array technology can thus quickly respond to customer requirements in a low cost and efficient manner. Gate arrays can be implemented using a variety of circuit and process technologies including static CMOS and bipolar emitter coupled logic.

Summary

The invention provides a monotonic dynamic-static pseudo-NMOS logic circuit. The monotonic dynamic-static pseudo-NMOS logic circuit includes a dynamic logic circuit having a clock input and having an output configured to be pre-charged high when a low clock signal is provided to the clock input. The monotonic dynamic-static pseudo-NMOS logic circuit further includes a static logic circuit having a clock bar input and having an output configured to be precharged

low when a high value of the complement of the clock signal is provided to the clock bar input.

In one aspect of the invention, the static logic circuit has a logic input coupled to the output of the dynamic logic circuit. In another aspect of the invention, the dynamic logic circuit has a logic input coupled to the output of the static logic circuit.

In one aspect of the invention, the dynamic logic circuit includes a p-type transistor having a control electrode defining the clock input and has a channel extending between a voltage supply and the output of the dynamic logic circuit. The dynamic logic circuit further comprises logic circuitry, configured to define a logic function, coupled between a low voltage and the output configured to be precharged high.

In another aspect of the invention, the static logic circuit includes a p-type transistor having a control electrode defining the clock input and having a channel extending between a voltage supply and the output of the static logic circuit. The static logic circuit further comprises logic circuitry, configured to define a logic function, coupled between a low voltage and the output configured to be precharged low.

Another aspect of the invention provides a logic gate array comprising a plurality of vertical ultrathin transistors coupled together.

Brief Description of the Drawings

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a circuit schematic showing a conventional static CMOS logic circuit.

Fig. 2 is a circuit schematic showing a low skew NAND of monotonic CMOS logic circuit.

Fig. 3 is a circuit schematic showing a high skew NAND of the monotonic CMOS logic circuit.

Fig. 4 is a circuit schematic of a pseudo-NMOS static logic circuit.

Fig. 5 is a circuit schematic of a zipper-CMOS logic circuit.

Fig. 6 is a circuit schematic showing a dynamic portion of monotonic dynamic-static pseudo-NMOS logic circuit.

Fig. 7 is a circuit schematic showing a static portion of the monotonic dynamic-static pseudo-NMOS logic circuit.

Fig. 8 is a block diagram representation of the circuit of Fig. 6.

Fig. 9 is a block diagram representation of the circuit of Fig. 7.

Fig. 10 is a circuit schematic illustrating multiple circuits of the type shown in Figs. 6 and 7 coupled together.

Fig. 11 is a perspective view of a semiconductor wafer illustrating steps in a process for manufacturing transistors for the circuits of Fig. 6 or Fig. 7.

Fig. 12 is a front elevational view of the wafer of Fig. 11.

Fig. 13 is a front elevational view of the wafer of Fig. 12 after a subsequent processing step.

Fig. 14 is a front elevational view of the wafer of Fig. 13 after a subsequent processing step.

Fig. 15 is a front elevational view of the wafer of Fig. 14 after a subsequent processing step.

Fig. 16 is a top plan view of a wafer after a step subsequent to a step such as the one illustrated in Fig. 15.

Fig. 17 is a front elevational view of the wafer of Fig. 16.

Best Modes for Carrying Out the Invention and Disclosure of Invention

Fig. 1 shows a prior art static CMOS logic circuit 10. A problem with static CMOS logic circuits is that each input 12 and 14 must drive two gates, the gate of one NMOS transistor and the gate of a PMOS transistor. Input 12 drives gates 16 and 18, and input 14 drives gates 20 and 22. This results in a large area for static CMOS circuits and a large number of metal wiring levels must be utilized to allow interconnections.

Another problem with static CMOS logic circuits is that in the PMOS transistor the hole mobility is about three times lower than the mobility of electrons if the transistors have comparable sizes. Because of this, switching transients are very asymmetrical. The charge up transient of the capacitive load in a simple inverter takes far longer than the discharge transient. To attempt to compensate, the PMOS transistors are often fabricated with a large width or size to provide symmetrical switching. However, this increases the stray capacitive loads and results in an even larger area for the circuits, and very inefficient area utilization.

Figs. 2 and 3 show monotonic static CMOS logic circuits (logic gates) 24 and 40. The circuit 24 is a low skewed logic circuit having devices which are sized so that the logic circuit 24 has a fast fall delay at the expense of a slow rise delay. The circuit 40 is a high skewed logic circuit designed to provide a fast pull-up.

The circuit 24 has inputs 26 and 28. The input 26 drives gates 30 and 32 and the input 28 drives gates 34 and 36. The circuit 40 has inputs 42 and 44. The input 42 drives gates 46 and 48 and the input 44 drives gates 50 and 52. A clock input CLK is provided to a gate 40 of the circuit 24 and a complementary clock signal CLK BAR is provided to a gate 56 of the circuit 40. When CLK is low, the output of the logic circuit 24 is precharged to a logic 1 and the output of the logic circuit 40 is precharged to a logic 0. During the evaluation phase of CLK, the output of the logic circuit 24 with either switch from 1 to 0 or remain at the precharged value. Similarly, the output of the logic circuit 40 will either switch from 0 to 1 or remain at the precharged value. A path of monotonic static logic circuits must alternate with low skewed and high skewed logic circuits. A low skewed logic circuit drives a high skewed logic circuit and vice versa.

Monotonic static CMOS logic circuits are known in the art and are discussed, for example, in T. Thorp, G. Yee and C. Sechen, "Monotonic Static CMOS and Dual VT Technology," Int. Sym. Low Power Electronics and Design, San Diego, 16-17 Aug. 1999, pp 151-155. In the circuit 24, the large charge up time through the PMOS devices is avoided by precharging output node 38 to VDD by the use of the clock, CLK. When the clock CLK is low, the PMOS transistor 40 will be on and the output load capacitance will be precharged to VDD. Similarly, in the complementary logic circuit 40 (Fig. 3), the complementary clock voltage CLK BAR will be high and the output 54 precharged to a low voltage or ground.

The outputs of the logic circuits are preset (precharged) high (for a pull-down circuit 24) or low (for a pull-up circuit 40), and hence the logic circuits either stay with that output value or switch to the other during evaluation. This is called monotonic behavior. For example, the only possible output transitions for a pull-down logic circuit are 0 to 0, 1 to 1, and 0 to 1. This is in contrast to regular static CMOS circuits, in which an output can perform any of the following transitions: 0-0, 1-1, 0-1, and 1-0. The logic circuits 24 and 40 are cascaded with one of the first type, then one of the second type, then one of the first type, etc.

More particularly, the logic circuit 24 is a low skew NAND. When CLK is low, logic circuit 24 is precharged high. Evaluation in circuit 24 takes place when CLK is high. The output 38 switches from 1 to 0 or remains. The logic circuit 40 is a high skew NAND. When CLK is low, CLK BAR is high, and circuit 40 is precharged low. Evaluation in circuit 40 takes place when CLK is high (CLK BAR is low). The output 54 switches from 0 to 1 or remains the same.

By an appropriate logic optimization of the inputs and arrangement of the circuits, the circuits can be placed so as to minimize signal delays through the circuit and minimize power consumption. This is possible because the circuit nodes are precharged prior to any of the input data becoming high and a monotonic logic evaluation of these inputs to the circuit. The sizes of the devices can be optimized to quickly discharge the charged nodes and quickly charge the discharged nodes. A 1.5 times speed improvement and a 1.5 times area reduction has been demonstrated over conventional static CMOS logic.

With respect to synthesis and logic optimization, attention is directed towards T. Thorp, G. Yee and C. Sechen, "Monotonic Static CMOS and Dual VT Technology," Int. Sym. Low Power Electronics and Design, San Diego, 16-17 Aug. 1999, pp 151-155. That article indicates that monotonic logic is non-inverting and must be mapped to a network that does not contain intermediate inversions. The removal of intermediate inverters within a logic network can be accomplished by generating a unate representation for the network, which may require logic duplication because separate logic cones for both positive and negative signal phases may be needed. After a unate representation has been generated, the network can be mapped to monotonic static CMOS gates using, for example, a concurrent two-coloring and technology mapping algorithm to merge a unate network's non-inverting functions into an alternating pattern of low skew and high skew logic gates. See T. Thorp, G. Yee, and C. Sechen, "Domino logic synthesis using complex static gates," IEEE/ACM Int. Conf. On Computer-Aided Design, pp. 242-247, 1998. The following two-coloring and mapping algorithm is indicated by Yee and Sechen as being useful when it is desired that each low skew gate will have no pull-down path longer than a user specified limit and that each high skew gate will have non pull-up path longer than a user specified limit:

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procedure
    while performing a postorder traversal of a network N from its outputs
        for all predecessors of current_node that are not multi-output nodes
            predecessor_node=current_node's predecessor with
            a) the greatest distance from a primary input and, to break ties,
            b) the fewest number of transistors in series;
            if merging predecessor_node and current_node satisfy node limits
                merge predecessor with current node;
            update node colors;
            resolve color conflicts;
end procedure
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Fig. 4 shows a pseudo NMOS static logic circuit 58. The circuit 58 shown in Fig. 4 includes circuitry 59 defining a logic function. While the circuitry 59 is used to define a two input NAND, different logic functions could be implemented. In a pseudo NMOS static logic circuit, the PMOS devices act as load devices, much like as depletion mode load devices in an enhancement-depletion NMOS static logic circuit. Although wiring complexity is significantly reduced, a difficulty is with static DC power consumption. Static DC power consumption can be avoided by using clocked sequential dynamic logic families like domino CMOS or NORA (no race) dynamic logic, or a combination of dynamic and static logic. Other circuit techniques include zipper CMOS and sequentially clocked or clock-delayed logic circuits.

Fig. 5 shows a zipper CMOS logic circuit 60. The circuit 60 includes logic circuitry 62, 64, and 66 defining logic functions. The circuit 60 has inputs 68, 70, 72, 74, 76, and 78, and outputs 80, 82, and 84. In the zipper CMOS logic circuit 60, the precharge phase is when the clock CLK is low (the complement CLK BAR is high). Evaluation occurs when the clock, CLK, goes low. The signals and logic decisions propagate through a chain defined by logic circuitry 62, 64, and 66 like a mechanical zipper closing, hence the name zipper CMOS.

Zipper CMOS, pseudo NMOS, and domino logic circuits are described, for example, in the following U.S. patents, all of which are incorporated herein by reference: 6,108,805 to Rajsuman; 6,107,835 to Blomgren et al.; 5,973,514 to Kuo et al.; 5,942,917 to Chappell et al.; 5,828,234 to Sprague; 5,867,036 to Rajsuman;

5,798,938 to Heikes et al.; 5,796,282 to Sprague et al.; 5,550,487 to Lyon; 5,525,916 to Gu et al.; 4,797,580 to Sunter; 4,569,032 to Lee.

Figs. 6 and 7 show monotonic static CMOS logic circuits (or logic gates, cells, blocks, or stages) 100 and 102 in accordance with one aspect of the invention. The circuit 100 has logic circuitry 103. The illustrated logic circuitry 103 inputs 104, 106, and 108. Circuitry configured to perform any one of multiple possible logic functions could be substituted for the logic circuitry 103. The circuit 100 also includes a clock input 110 coupled to a source of a clock signal CLK, and an output 112. The circuit 100 is a dynamic circuit which is precharged high at the output 112. The circuit 100 is precharged high at the output 112.

The circuit 102 has logic circuitry 113. The illustrated logic circuitry 113 has inputs 114, 116, and 118. Circuitry configured to perform any one of multiple possible logic functions could be substituted for the logic circuitry 113. Figs. 6 and 7 show three input NOR logic circuitry for circuitry 103 and 113, but other numbers of inputs or an inverter can be implemented by using a different number of transistors in circuitry 103 and 113. The circuit 102 also includes a clock input 120 coupled to the source of the clock signal CLK of Fig. 6, an input 122 coupled to the complement (CLK BAR) of the clock signal CLK of Fig. 6, and an output 124. The circuit 102 is precharged low at the output 124.

Figs. 8 and 9 are simplified block diagram representations of the circuits 100 and 102, respectively.

Circuits such as the circuits 100 and 102 are configured to be coupled together in sequence in an alternating fashion; e.g., one high precharge circuit (e.g., circuit 100), one low precharge circuit (e.g., 102), one high precharge circuit, one low precharge circuit, and so on (see, e.g., Fig. 10). The circuits 100 and 102 are precharged when the clock CLK is low (the complement CLK BAR is high). Following the precharge, some or all of the inputs 104, 106, 108, 114, 116, 118, 122 can change state and monotonic evaluation of the input will be performed by the logic circuits 100 and 102.

The outputs 112 and 124 of the logic circuits are preset (precharged) high for pull-down circuits (e.g. 100) and preset (precharged) low for pull-up circuits (e.g. 102). Therefore the logic circuits 100 and 102 either retain that output value (0 or 1) or switch to the other value during evaluation. This is monotonic behavior. Because the first stage is dynamic and the next stage is static during the evaluation

phase, a circuit family including circuits 100 and 102 is most appropriately referred to as a monotonic dynamic-static pseudo-NMOS.

As is the case with monotonic static CMOS logic, the inputs and arrangement of the circuits 100 and 102 can be arranged to minimize signal delays through the circuit, and to minimize power consumption, using synthesis techniques known in the art and described, for example, in T. Thorp, G. Yee and C. Sechen, "Monotonic Static CMOS and Dual VT Technology," Int. Sym. Low Power Electronics and Design, San Diego, 16-17 Aug. 1999, pp 151-155 (see above). This is possible because the circuit nodes are precharged prior to any of the input data becoming high and prior to a monotonic logic evaluation of these inputs to the circuit. In one embodiment, the device sizes are optimized to quickly discharge the charged nodes and quickly charge the discharged nodes.

In a monotonic dynamic-static pseudo-NMOS including circuits 100 and 102, the second stage is static during the evaluation phase and uses NMOS devices for the evaluation. This is in contrast, for example, to zipper-CMOS where PMOS devices are used in the second stage. The use of NMOS devices in applicant's monotonic dynamic-static pseudo-NMOS results in a faster switching speed, though at the expense of some DC power dissipation. The monotonic dynamic-static pseudo-NMOS including circuits 100 and 102 uses far fewer devices, much less area, and much less wiring than domino static-CMOS logic configurations.

While full rail CMOS voltages, such as 5 volts and ground, could be used to define the high and low voltages, in other embodiments, different voltages are used as will be readily apparent to one of ordinary skill in the art. For example, 4 volts and 1 volts could be used to define the high and low voltages, respectfully; anything above a certain threshold could be considered high and anything below a certain threshold could be considered low, or a negative voltage could be used for the low voltage or for both the high and low voltages. As long as the high and low voltages can be distinguished from one another with sufficient reliability for the specific application, any voltages can be used to define the high and low voltages.

Process Technology Embodiments

The continuous scaling of MOSFET technology to reduce channel lengths to, for example, the deep sub-micron region where channel lengths are less than 0.1 micron, 100 nm, or 1000A causes significant problems in the conventional transistor

structures. Junction depths should be much less than the channel length. This implies junction depths of a few hundred Angstroms for channel lengths of 1000 Angstroms. Such shallow junctions are difficult to form by conventional implantation and diffusion techniques. Extremely high levels of channel doping are required to suppress short-channel effects such as drain induced barrier lowering, threshold voltage roll off, and sub-threshold conduction. Sub-threshold conduction is particularly problematic in dynamic circuits technology because it reduces the charge storage retention time on capacitor nodes. These extremely high doping levels result in increased leakage and reduced carrier mobility. Therefore, the improved performance by making the channel shorter is negated by lower carrier mobility.

What is required, then, are transistors with ultra-thin bodies, or transistors where the surface space charge region scales down as other transistor dimensions scale down. Raising or burying the source/drain contact regions above or below the channel allows contacts to be made by conventional techniques.

In the embodiment shown in Figs. 11-12, a silicon semiconductor substrate 202 is first provided. The substrate 202 can be any of three different types of substrates:

(i) lightly doped p-type;

(ii) conventional commercial silicon on insulator substrates (e.g. SIMOX); or

(iii) islands of silicon on insulator formed by techniques such as those described in U.S. Patent No. 5,691,230 to Forbes, incorporated herein by reference.

SIMOX (Separation by IMplanted Oxygen) involves implanting a high dose of oxygen ions at a sufficiently deep level within a silicon substrate. A subsequent anneal step forms a buried oxide layer in the substrate. After the anneal step, an additional layer of epitaxial silicon is usually deposited to obtain a sufficiently thick silicon layer on which to form a device.

A substrate of islands of silicon on insulator can be formed, for example, by directionally etching a silicon substrate, to form a plurality of trenches between protruding silicon rows; forming a silicon nitride cap on the silicon rows, extending partway down the sides of the trenches; isotropically etching the trenches, to partially undercut the silicon rows; and oxidizing the substrate, to fully undercut the silicon rows.

In the embodiment shown in Figs. 11-15, the substrate 202 is of p-type material.

An ultrathin body transistor 200 is fabricated by oxidizing the silicon semiconductor substrate 202, and then etching pillars of oxide 204 into the substrate 202. The oxidized wafers previously had a layer of doped polysilicon deposited on the oxide. Layers of oxide and silicon nitride are deposited to act as an etch mask for forming the pillars and later as a CMP etch stop. In the embodiment shown in Figs. 11 and 12, layer 206 is formed of n+ material, layer 208 is formed of p+ material. Layers 206 and 208 can be formed on the substrate, for example, by ion implantation or epitaxial growth. Layer 210 is oxide. Upper layers 212 are formed of n+ material, and upper layers 214 are formed of p+ material. These process steps are described in greater detail in U.S. Patent No. 6,072,209 to Noble et al., and in U.S. Patent No. 6,150,687 to Noble et al., both of which are incorporated herein by reference.

As shown in Figs. 13-15, transistors with ultra-thin bodies are formed along side of respective oxide pillars 204. In Fig. 13, polysilicon 216 is deposited over the silicon pillars 204 and directionally etched to leave the lightly doped p-type material on the sidewalls of the pillars.

At this point, another masking step can be employed (see Fig. 14) to isotropically etch the polysilicon 216 off of some of the sidewalls 218 and 220 and leave polysilicon only on one sidewall 222 and 224 of each pillar as required for particular configurations.

Then, (see Fig. 15) the wafer is heated at about 550°C to about 700°C and the polysilicon will recrystallize and lateral epitaxial solid phase regrowth will occur vertically as indicated by arrows 226 and 228. The crystalline silicon at the bottom will seed this crystal growth and an ultrathin crystalline film will form on each pillar 204 that can be used as the channel of a MOSFET transistor. If the film is only on one side 222 of the pillar 204, the crystallization will proceed vertically and into the n+ polysilicon contact material 212 on top of the pillar 204. If both sides of the pillar are covered, the crystallization will leave a grain boundary near the center on top of the pillar 204.

These techniques are similar, in part, to techniques described (in connection with different applications) in P Xuan et al., 60nm Planarized Ultra-thin Body Solid Phase Epitaxy MOSFETs, IEEE Device Research Conf., Denver, CO, June 2000, pp.

67-68, and in P. Kalavade et al, A Novel Sub-10nm Transistor, IEEE Device Research Conf., Denver, CO, June 2000, pp. 71-77.

The drain and source regions of a transistor are in the crystalline material along the sidewall of each pillar 204. A gate insulator is grown or deposited on this thin film and either a horizontal or vertical gate structure is formed in the trench beside the pillar 204. Horizontal gate structures for use with vertical pillar transistors are described, for example in incorporated U.S. Patent No. 6,150,687 to Noble et al. or in U.S. Patent Application Serial No. 09/596,266 filed June 16, 2000 naming as inventors Noble, Forbes, and Ahn, and incorporated herein by reference. The different gate structures used in alternative embodiments are therefore:

(i) horizontal gate structures of deposited polisilicon, as described in U.S. Patent No. 6,150,687 to Noble et al.;

(ii) horizontal replacement gate structures, a variation on U.S. Patent No. 6,150,687, described in U.S. Patent Application Serial No. 09/596,266 filed June 16, 2000; and

(iii) vertical gate structures as described in U.S. Patent No. 6,072,209 to Noble et al.

Figs. 16 and 17 illustrate the implementation of a logic gate using vertical devices.

The logic gate implemented in Figs. 16 and 17 is a dynamic three-input NOR gate, similar to the circuit 100 of Fig. 6 (except without the capacitor being specifically illustrated). However, it will be readily apparent that any logic gate can be implemented using vertical devices.

The configuration shown in Figs. 16 includes contacts 230, 232, 234, and 236 defining inputs 104 (or A), 106 (or B), 108 (or C), and 110 (or CLK), respectively of Fig. 6. Contacts 238 and 240 are coupled together to define the output 112. Contacts 242 and 244 are also included.

The configuration shown in Fig. 17 includes oxide areas 204, 210, 246; thick oxide areas 248 and 250, n+ areas 206, and 212, an area 252 of poly, areas 254 and 256 of silicon , and gate oxide area 258.

One of the differences between the illustrated implementation and the incorporated prior patents and application is the thick oxide formed along side one of the vertical walls of a pillar 204. Another difference is the utilization of both PMOS and NMOS vertical devices in the array. Three different types of gate

structures have been described, and these can be utilized on three different disclosed types of substrates to form the gate arrays.

Higher and higher density requirements in logic gates result in smaller and smaller dimensions of the structures and included transistors. Conventional planar transistor structures are difficult to scale to deep sub-micron sizes. Applicant has provided vertical transistors with ultrathin bodies in connection with logic gate arrays. The advantages of smaller dimensions for higher density and higher performance are both realized in logic gate arrays by employing vertical ultrathin transistors in logic gate arrays.

CLAIMS

1. A monotonic dynamic-static pseudo-NMOS logic circuit comprising:

a dynamic logic circuit having a clock input and having an output configured to be pre-charged high when a low clock signal is provided to the clock input; and

a static logic circuit having a clock bar input and having an output configured to be precharged low when a high value of the complement of the clock signal is provided to the clock bar input, the static logic circuit having a logic input coupled to the output of the dynamic logic circuit.

2. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 1 wherein the dynamic logic circuit includes a p-type transistor having a control electrode defining the clock input and has a channel extending between a voltage supply and the output of the dynamic logic circuit.

3. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 2 wherein the dynamic logic circuit further comprises logic circuitry, configured to define a logic function, coupled between a low voltage and the output configured to be precharged high.

4. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 3 wherein the logic circuitry configured to define a logic function comprises a plurality of n-type transistors.

5. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 4 wherein the n-type transistors have respective gates which define inputs of the monotonic dynamic-static pseudo-NMOS logic circuit.

6. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 3 wherein the logic circuitry configured to define a logic function comprises a plurality of transistors, the transistors of the logic circuitry configured to define a logic function consisting essentially of n-type transistors.

7. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 6 wherein the n-type transistors have respective gates which define inputs to the logic circuitry.

8. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 4 wherein at least one of the transistors is a vertical ultrathin body transistor.

9. A monotonic dynamic-static pseudo-NMOS logic circuit comprising:

a dynamic logic circuit having a clock input and having an output configured to be pre-charged high when a low clock signal is provided to the clock input; and

a static logic circuit having a clock bar input and having an output configured to be precharged low when a high value of the complement of the clock signal is provided to the clock bar input, the static logic circuit having a logic input coupled to the output of the dynamic logic circuit, the static logic circuit including a p-type transistor having a control electrode defining the clock input and having a channel extending between a voltage supply and the output of the static logic circuit.

10. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 9 wherein the static logic circuit further comprises logic circuitry, configured to define a logic function, coupled between a low voltage and the output configured to be precharged low.

11. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 10 wherein the logic circuitry configured to define a logic function of the static logic circuit comprises a plurality of n-type transistors.

12. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 11 wherein the n-type transistors have respective gates which define inputs of the monotonic dynamic-static pseudo-NMOS logic circuit.

13. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 10 wherein the logic circuitry configured to define a logic function of the static logic circuit comprises a plurality of transistors, the transistors of the logic

circuitry configured to define a logic function consisting essentially of n-type transistors.

14. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 9 wherein the dynamic logic circuit includes a p-type transistor having a control electrode defining the clock input and has a channel extending between a voltage supply and the output of the dynamic logic circuit.

15. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 12 wherein at least one of the transistors is a vertical ultrathin body transistor.

16. A monotonic dynamic-static pseudo-NMOS logic circuit comprising:

a dynamic logic circuit having a clock input and having an output configured to be pre-charged high when a low clock signal is provided to the clock input; and

a static logic circuit having a clock bar input and having an output configured to be precharged low when a high value of the complement of the clock signal is provided to the clock bar input, the static logic circuit having a logic input coupled to the output of the dynamic logic circuit, the static logic circuit including a p-type transistor having a control electrode defining the clock input, having a channel extending between a voltage supply and the output of the static logic circuit, and having logic circuitry, configured to define a logic function, coupled between a low voltage and the output configured to be precharged low, wherein the logic circuitry configured to define a logic function includes a plurality of transistors, the transistors of the logic circuitry configured to define a logic function consisting essentially of n-type transistors having respective gates, one of which defines the clock bar input and the rest of which define inputs to the logic circuitry.

17. A monotonic dynamic-static pseudo-NMOS logic circuit comprising:

a static logic circuit having a clock bar input and having an output configured to be precharged low when a low clock signal is provided to the clock bar input; and

a dynamic logic circuit having a clock input, having an output configured to be pre-charged high when a low clock signal is provided to the clock input, having

a logic input coupled to the output of the static logic circuit, and having a p-type transistor including a control electrode defining the clock input, including a power electrode coupled to the voltage supply, and including a power electrode coupled to the output of the dynamic logic circuit.

18. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 17 wherein the dynamic logic circuit further comprises logic circuitry, configured to define a logic function, coupled between a low voltage and the output configured to be precharged high, the logic circuitry defining the logic input of the dynamic logic circuit.

19. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 18 wherein the logic circuitry configured to define a logic function comprises a plurality of n-type transistors.

20. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 19 wherein the n-type transistors have respective gates which define inputs of the monotonic dynamic-static pseudo-NMOS logic circuit.

21. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 18 wherein the logic circuitry configured to define a logic function comprises a plurality of transistors, the transistors of the logic circuitry configured to define a logic function consisting essentially of n-type transistors.

22. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 21 wherein the n-type transistors have respective gates which define inputs to the logic circuitry.

23. A monotonic dynamic-static pseudo-NMOS logic circuit comprising:

a static logic circuit having a clock bar input and having an output configured to be precharged low when a low clock signal is provided to the clock bar input; and

a dynamic logic circuit having a clock input and having an output configured to be pre-charged high when a low clock signal is provided to the clock input, the dynamic logic circuit having a logic input coupled to the output of the static logic circuit.

24. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 23 wherein the static logic circuit further comprises logic circuitry, configured to define a logic function, coupled between a low voltage and the output configured to be precharged low.

25. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 24 wherein the logic circuitry is coupled between ground and the output configured to be precharged low

26. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 24 wherein the logic circuitry configured to define a logic function of the static logic circuit comprises a plurality of n-type transistors.

27. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 26 wherein the n-type transistors have respective gates which define inputs of the monotonic dynamic-static pseudo-NMOS logic circuit.

28. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 24 wherein the logic circuitry configured to define a logic function of the static logic circuit comprises a plurality of transistors, the transistors of the logic circuitry configured to define a logic function consisting essentially of n-type transistors.

29. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 24 wherein the dynamic logic circuit includes a p-type transistor having

a control electrode defining the clock input and has a channel extending between a voltage supply and the output of the dynamic logic circuit.

30. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 29 wherein at least one of the transistors is a vertical ultrathin body transistor.

31. A monotonic dynamic-static pseudo-NMOS logic circuit comprising:

a static logic circuit having a clock bar input and having an output configured to be precharged low when a low clock signal is provided to the clock bar input, the static logic circuit further having logic circuitry, configured to define a logic function, coupled between a low voltage and the output configured to be precharged low, the logic circuitry configured to define a logic function of the static logic circuit including a plurality of transistors, the transistors of the logic circuitry configured to define a logic function consisting essentially of n-type transistors, the n-type transistors having respective gates, one of which defines the clock bar input and the rest of which define inputs to the logic circuitry; and

a dynamic logic circuit having a clock input and having an output configured to be pre-charged high when a low clock signal is provided to the clock input, the dynamic logic circuit having a logic input coupled to the output of the static logic circuit.

32. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 31 wherein the dynamic logic circuit includes a p-type transistor having a control electrode defining the clock input and has a channel extending between a voltage supply and the output of the dynamic logic circuit.

33. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 32 wherein the dynamic logic circuit further comprises logic circuitry, configured to define a logic function, coupled between a low voltage and the output configured to be precharged high.

34. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 33 wherein the logic circuitry of the dynamic logic circuit comprises a plurality of n-type transistors.

35. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 34 wherein the n-type transistors of the logic circuitry of the dynamic logic circuit have respective gates which define inputs of the monotonic dynamic-static pseudo-NMOS logic circuit.

36. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 33 wherein the logic circuitry of the dynamic logic circuit comprises a plurality of transistors consisting essentially of n-type transistors.

37. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 36 wherein the n-type transistors have respective gates which define inputs to the logic circuitry.

38. A monotonic dynamic-static pseudo-NMOS logic circuit in accordance with claim 36 wherein at least one of the transistors is a vertical ultrathin body transistor.

39. A method comprising:

coupling the output of a dynamic logic circuit to a logic input of a static logic circuit, the dynamic logic circuit having a clock input; the static logic circuit having a clock bar input and having an output;

pre-charging high the output of the dynamic logic circuit when a low clock signal is provided to the clock input; and

precharging low the output of the static logic circuit when a high value of the complement of the clock signal is provided to the clock bar input.

40. A method comprising:

coupling the output of a static logic circuit to a logic input of a dynamic logic circuit, the dynamic logic circuit having a clock input; the static logic circuit having a clock bar input and having an output;

pre-charging high the output of the dynamic logic circuit when a low clock signal is provided to the clock input; and

precharging low the output of the static logic circuit when a high value of the complement of the clock signal is provided to the clock bar input.

41. A logic gate array comprising a plurality of vertical ultrathin transistors coupled together.

42. A method of forming a logic gate array comprising:

providing a substrate having a generally planar working surface;

oxidizing the substrate;

forming a pillar of semiconductor material extending outwardly from the working surface of the substrate, the pillar having a plurality of sidewalls;

depositing polysilicon over the pillars;

directionally etching the deposited polysilicon;

heating to cause lateral epitaxial solid phase regrowth vertically to form a thin film defining first and second source/drain regions of a transistor;

forming a gate insulator on the thin film; and

forming a gate structure relative to the thin film.

43. A method in accordance with claim 42 wherein providing a substrate comprises providing a lightly doped p-type substrate.

44. A method in accordance with claim 42 wherein providing a substrate comprises providing a silicon on insulator substrate.

45. A method in accordance with claim 42 wherein providing a substrate comprises providing islands of silicon on insulator.

46. A method in accordance with claim 42 wherein forming a gate structure comprises forming a horizontal gate structure.

47. A method in accordance with claim 42 wherein forming a gate structure comprises forming a horizontal replacement gate structure.

48. A method in accordance with claim 42 wherein forming a gate structure comprises forming a vertical gate structure.

49. A method of forming a logic gate array comprising:

providing a substrate having a generally planar working surface;

forming a plurality of pillars of semiconductor material extending outwardly from a working surface of the substrate, the pillar having a plurality of sides; and

forming a plurality of vertical transistors having first and second source/drain regions formed within one of the pillars and having a gate associated with a side of that pillar, wherein one of the vertical transistors is a PMOS transistor and another of the transistors is an NMOS transistor.