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DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Signal Translating Circuits

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to signal translating circuits employing an insulated gate field-effect semiconductor device, e.g. a transistor.

An insulated gate field-effect transistor is a field-effect transistor having a gate electrode which is insulated from the source and drain electrodes. These transistors have (1) high input impedance, (2) low cross modulation, (3) bilateral conduction, (4) low noise, (5) simplified direct coupling capability, and (6) compatibility with integrated circuit techniques.

It has been found that signal translating circuits using insulated gate field-effect transistors may exhibit stability problems when operated at high frequencies. Ordinarily high frequency signal translating circuits using transistors or vacuum tubes may be stabilized by using the so-called common-base or grounded grid connections to reduce feedback between the input and output circuits. However, operation of the insulated gate field-effect transistor in the common-gate mode may not correct the stability problem, and the circuit has been operated at low gain to maintain stability.

In addition to the foregoing problem, it has been found that distortion may occur at some signal levels particularly when a field-effect transistor is used in the so-called "cascode" amplifier.

Accordingly, it is an object of this invention to provide a new and improved signal translating circuit employing an insulated gate field-effect semiconductor device.

A signal translating circuit according to one aspect of this invention comprises: a field-effect semiconductor device with source, gate and drain electrodes formed on a substrate of semiconductor material, the gate electrode being insulated from the substrate; circuit means connecting the device as the active element of a signal translating circuit with one of the source, gate and drain electrodes as an input electrode, a second one of said source, gate and drain electrodes as an output electrode, and the remaining one of the source, gate and drain electrodes being a common electrode; other circuit means providing a point of relatively fixed potential for said signal translating circuit referenced with respect to the common electrode; and means for connecting the substrate to the point of fixed potential.

A signal translating circuit according to another aspect of this invention comprises first and second field-effect transistors each having source and drain electrodes, said electrodes being formed on a single substrate of semiconductor material, each said transistor having a gate electrode insulated from said substrate, and said source and drain electrodes of said first and second field-effect transistors each being effectively coupled to said substrate by a rectifying junction poled so that a positive potential applied to said substrate with respect to the potential of the corresponding one of said source and drain electrodes renders said rectifying junction conductive; means connecting the source-to-drain current paths of said first and second field-effect transistors in series; means for applying a bias potential across the series combination of said source-to-drain current paths of said first and second field-effect transistors; circuit means for bias-

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ing said gate electrodes to predetermined bias potentials; capacitative means coupling the gate electrode of said first field-effect transistor to the source electrode of said second field-effect transistor to provide an alternating current point of reference potential to said gate electrode of said first field-effect transistor; input circuit means coupled between the gate and source electrodes of said second field-effect transistor for applying input signals to said amplifier circuit; output circuit means coupled to the drain electrode of said first field-effect transistor for deriving output signals; and means coupling said substrate to said source electrode of said second field-effect transistor to prevent energy from feeding back from said output circuit to said input circuit.

The invention will now be described with reference to the accompanying drawings, in which:

FIGURE 1 is a diagrammatic plan of an insulated gate field-effect transistor suitable for use in circuits embodying the invention;

FIGURE 2 is a cross section view taken along line 2—2 of FIGURE 1;

FIGURE 3 is a symbolic representation of an insulated gate field-effect transistor;

FIGURE 4 is a graph showing a family of drain current versus source-to-drain voltage curves for various values of gate-to-source voltages for the transistors of FIGURES 1 and 2;

FIGURE 5 is a schematic circuit diagram of a signal translating circuit embodying the invention;

FIGURE 6 is a schematic circuit diagram of a cascode amplifier circuit embodying the invention;

FIGURE 7 is a perspective view, partially in cross section, of a pair of insulated gate field-effect transistors having a common substrate which may be used in circuits embodying the invention;

FIGURE 8 is a perspective view, partially in cross section, of still another insulated gate field-effect transistor which may also be used in circuits embodying the invention; and

FIGURE 9 is a perspective view, partially in cross section, of an insulated gate field-effect transistor having two gate electrodes and a single conductive channel.

Referring particularly to FIGURE 1, a field-effect transistor 10 which may be used with circuits embodying the invention includes a substrate or a body 12 of semiconductor material. The body 12 may be either a single crystal or polycrystalline and may be of any of the semiconductor materials used to prepare transistors in the semiconductor art. For example, the body 12 may be nearly intrinsic silicon, such as lightly doped P-type silicon of 100 ohm-cm. material.

In the manufacture of the device shown in FIGURE 1 heavily doped silicon dioxide is deposited over the surface of the silicon body 12. The silicon dioxide is doped with N-type impurities. By means of a photo-resist and acid etching, or other suitable technique, the silicon dioxide is removed where the gate electrode is to be formed, and around the outer edges of the silicon wafer as viewed on FIGURE 1. The deposited silicon dioxide is left over those areas where the source and drain regions are to be formed.

The body 12 is then heated in a suitable atmosphere, such as in water vapour, so that exposed silicon areas are oxidized to form grown silicon dioxide layers indicated by the lightly stippled areas of FIGURE 1. During the heating process, impurities from the deposited silicon dioxide layer diffuse into the silicon body 12 to form respectively the source and drain regions. FIGURE 2 shows the source and drain regions labelled *S* and *D* respectively.

By means of another photo-resist and acid etching or like step, the deposited silicon dioxide over part of the source and drain diffused regions is removed. Electrodes are formed for the source, drain and gate regions by evaporation of a conductive material by means of an evaporation mask. The conductive material evaporated may be chromium and gold in the order named, for example, but other suitable metals may be used.

The finished wafer is shown in FIGURE 1, in which the lightly stippled area between the outside boundary and the first darker zone 14 is grown silicon dioxide. The white area 16 is the metal electrode corresponding to the source electrode. Darker or more heavily stippled zones 14 and 18 are deposited silicon dioxide zones overlying the diffused source regions, and the dark zone 20 is a deposited silicon dioxide zone overlying the diffused drain region. White areas 22 and 24 are the metallic electrodes which correspond to the gate and drain electrodes respectively. The lightly stippled zone 28 is the gate region which is a layer of grown silicon dioxide on a portion of which the gate electrode 22 is evaporated.

The silicon wafer is mounted on a conductive base or header 26 as shown in FIGURE 2. The input resistance of the device at low frequencies is of the order of 10^{14} ohms. The gate region 28, on which the gate electrode 22 is mounted, overlies an inversion layer or conductive channel *C* connecting the source and drain regions. The gate electrode 22 is arranged symmetrically between the source region S and the drain region *D*. If desired, the gate electrode 22 may be arranged closer to the source region and may overlap the deposited silicon dioxide layer 18.

Reference is now made particularly to FIGURE 2. The boundaries separating the source and drain regions *S* and *D* and the body of silicon substrate 12 effectively operate as a pair of rectifying junctions coupling the

silicon substrate 12 to the source and drain electrodes 16 and 24, in such a manner that a positive bias voltage applied to the substrate with respect to the drain and source electrodes 16 and 24 renders the rectifying junction conductive, i.e. forward biased.

The poling of the rectifying junctions described is representative of a transistor of the type described in connection with FIGURES 1 and 2 where the substrate is of P-type material relative to the source and drain electrodes. However, the transistor device can be fabricated with an N-type material substrate relative to the source and drain electrodes. In devices of the latter type, the rectifying junctions would be poled so that the anode side of the rectifying junction appears at the source and drain electrodes, and the cathode side of these junctions appears at the substrate. The devices shown in the subsequent FIGURES will be of the type of device described in connection with FIGURES 1 and 2 wherein the substrate is of P-type relative to the source and drain electrodes.

FIGURE 3 is a symbolic representation of the insulated gate field-effect transistor previously described in FIGURES 1 and 2. There is shown the gate electrode G, the drain electrode D, the source electrode S, and the substrate of semiconductor material S_u. It should be noted that electrodes D and S operate as the drain and source electrodes as a function of the polarity of the bias potential applied therebetween; i.e. the electrode to which a positive bias potential is applied (relative to the bias potential applied to the other electrode) operates as a drain electrode, and the other electrode operates as a source electrode.

The drain and source electrodes are connected to each other by a conductive channel C. The majority current carriers (in this case electrons) flow from source to drain in this thin channel region close to the surface. The conductive channel C is shown in FIGURE 2 in dotted lines.

FIGURE 4 displays a family of curves 30—39 illustrating the drain current versus drain voltage characteristic of the transistor of FIGURE 1 for different values of gate-to-source voltage. A feature of an insulated gate field-effect transistor is that the zero bias characteristic can be at any of the curves 30—39. In FIGURE 4 the curve 37 corresponds to the zero bias gate-to-source voltage. Curves 38 and 39 represent positive gate voltages relative to the source, and the curves 30—36 represent negative gate voltages relative to the source.

The location of the zero bias curve is selected during the manufacture of the transistor, i.e. by controlling the time or the temperature, or both, during the step of the process in which the silicon dioxide layer 28, shown in FIGURES 1 and 2, is grown. The longer the transistor is baked and the higher the temperature in a dry oxygen atmosphere the larger the drain current will be for a given amount of drain voltage at zero bias between the source and gate electrodes.

Reference is now made to FIGURE 5, which is a schematic diagram of an amplifier circuit employing an insulated gate field-effect transistor 50 similar to the transistor illustrated in FIGURES 1 and 2. The transistor 50 has an input or source electrode 52, an output or drain electrode 54, a common or gate electrode 56, and a substrate 58 of semiconductor material. The input and output electrodes 52 and 54 operate as the source and drain electrodes in accordance with the polarity of the potential applied between them. That is, the electrode which has a positive potential applied thereto with respect to the potential of the other electrode operates as the drain electrode.

A source of input signals 60, which comprises a generator signal source 62 and its internal resistance represented by the resistor 64, is coupled between the input electrode 52 and a point of reference potential, shown as ground, through a coupling capacitor 66. A resistor 67 references the input electrode 52 to ground. The common electrode 56 is connected through a resistor 68 to a source of bias potential E_1 which sets the operating point of the transistor. The common electrode 56 is maintained at reference or ground potential for signal frequencies by a capacitor 70. Coupling the common electrode 56 to ground reduces the signal feedback through the intrinsic capacitance of the field-effect transistor 50 between the output electrode and the input electrode.

A pair of rectifying junctions 72 and 74 exist between the substrate 58 of semiconductor material and the input and output electrodes 52 and 54 respectively. The pair of rectifying junctions 72 and 74 are poled in such a manner that a positive voltage applied to the substrate with respect to the potential applied to the input or output electrodes 52 or 54 renders the rectifying junctions 72 and 74 conductive. The rectifying junctions 72 and 74 have intrinsic capacitance, which in this particular case provides a feedback path between the input and output circuits.

The substrate 58 of semiconductor material is directly connected to ground. Energy transfer between the input and output circuits by way of the substrate is thereby reduced, and the intrinsic capacitative voltage divider circuit (between the input and output electrodes) is transformed into a pair of capacitors respectively connected between the input and output electrodes and ground.

An energizing voltage V_{SD} is coupled between the input and output electrodes through an inductor 76 from a source of bias potential (not shown) which may be a battery, for example. A bypass capacitor 78 is connected

between the low signal potential terminal of the inductor 76 and ground. Output signals are derived from the output electrode 54 and are coupled through a variable capacitor 80 to a utilization circuit (not shown).

In operation, a portion of the output signal derived from the output electrode 54 would ordinarily be fed back through the capacitative voltage divider network comprising the intrinsic capacitance of the rectifying junctions 72 and 74 if the substrate of semiconductor material 58 were not grounded. Grounding the substrate of semiconductor material 58, however, reduces energy transfer from the ouput to the input circuit, and therefore provides stabilization of the circuit. Grounding the substrate also back biases the rectifying junctions 72 and 74 which results in a corresponding decrease of intrinsic capacitance of the rectifying junctions. In addition it divides the intrinsic capacitance by providing two separate paths to ground.

It should be understood that although the substrate 58 is shown directly connected to ground, the important consideration to reduce energy feedback from the output to the input electrodes of the field-effect transistor 50 is that the substrate 58 is direct current reverse biased with respect to the bias potential of both input and output electrodes 52 and 54, and that the substrate 58 is alternating current referenced. For example, the substrate 58 may be (1) connected to a voltage divider network comprising two resistors connected between the source of operating potential V_{SD} and ground, and (2) a-c coupled to ground through a capacitor exhibiting a low impedance at signal frequency and which is connected in parallel with one of the resistors of the voltage divider network to ground.

If the substrate 58 was left unconnected, signal distortion would occur. The rectifying junction 72, for example, would be rendered conductive, for a sufficiently large negative signal swing, causing signal clipping. Signal clipping is avoided by connecting the substrate 58 to a point of reference potential as previously described.

Reference is now made to FIGURE 6 which is a schematic circuit diagram of a cascode amplifier circuit employing insulated gate field-effect transistors 90 and 92 that are similar to the field-effect transistor illustrated in FIGURES 1 and 2. The field-effect transistors 90 and 92 have their source-to-drain current paths 94 and 96 connected in series by connecting the drain electrode 100 of the field-effect transistor 92 to the source electrode 102 of the field-effect transistor 90. The source electrode 98 is connected to a point of reference potential shown as ground.

Input signals are applied from a signal source (not shown) through a coupling capacitor 104 to the gate electrode 106 of the field-effect transistor 92. An output signal is derived from the drain electrode 108 of the field-effect transistor 90 and is coupled through a variable capacitor 110 into a utilization circuit (not shown). A direct voltage is applied between the drain electrode 108 of the field-effect transistor 90 and the source electrode 98 of the field-effect transistor 92 through an inductor 111 from a source of operating potential V_{SD} which may be a battery for example. A capacitor 112 bypasses the operating potential V_{SD} for signal frequencies. The gate electrodes 118 and 106 of the field-effect transistors 90 and 92 are respectively biased with respect to the source electrodes 102 and 98 from sources of bias potential E_1 and E_2 through resistors 114 and 116. The gate electrode 118 of the field-effect transistor 90 is coupled to ground for signal frequencies by means of a capacitor 120.

A pair of rectifying junctions 122 and 124 exist between the substrate 126 of semiconductor material of the field-effect transistor 90 and the drain and source electrodes 108 and 102 respectively. Similarly, a pair of rectifying junctions 128 and 130 exist between the substrate 132 of semiconductor material and the drain and source electrodes 100 and 98 of the field-effect transistor 92. The rectifying junctions 122, 126, 128 and 130 are poled so that their anodes are at the substrates 126 and 132 respectively.

By connecting the substrates of semiconductor material 126 and 132 to ground, isolation between the input and output electrodes, and thereby stabilization of the amplifier circuit, is provided. The input stage of the amplifier circuit (which includes the field-effect transistor 92 as the active element) is stabilized by the loading caused by the low input impedance of the output stage (which includes the field-effect transistor 90 as the active element). The reason why the input impedance of the common-gate stage is low is that the input impedance includes the resistance exhibited by the source-drain current path which is in the order of hundreds of ohms, in comparison to the high input impedance (10^{14} ohms) of the common-source configuration.

The output stage of the amplifier circuit is stabilized by means of the capacitor 120 which provides an alternating current ground for the gate electrode 118, to isolate the output and input electrodes 108 and 102, and thereby reduce energy transfer through the intrinsic capacitance between the gate electrode and the output and input electrodes respectively. However, the intrinsic capacitance of the rectifying junctions 122 and 124 provides another feedback path which creates instability problems. Energy feedback through the rectifying junctions is reduced by grounding the substrate 126 of semiconductor material to effectively provide a shield between the output and input electrodes 108 and

102. Grounding the substrates 126 and 132 also reduces the capacitance of the rectifying junctions 122, 124, 128 and 130 because the rectifying junctions are thereby back-biased.

If the substrates 126 and 132 were left unconnected, distortion of the output signal would occur. For example, when the signal appearing at the source electrode 102 swings negatively with respect to the voltage at the substrate 126, the rectifying junction 124 would be rendered conductive causing rectification of the signal. Similarly, rectifying junction 128 may cause rectification or clipping of the signals. This is because the substrate 132 tends to assume the average positive potential of the drain electrode 100 through the back resistance of the rectifying junction 128. Thus, if the drain electrode 100 swings sufficiently in the negative direction, the rectifying junction 128 conducts causing signal clipping.

By grounding both substrates 126 and 132 the rectifying junctions are maintained in a back biased condition so that distortion of the output signal is avoided. If desired, the circuit of FIGURE 6 may be altered to zero-bias operation of the field-effect transistor 90 by connecting the resistor 114 between the gate and the source electrodes 118 and 102.

The gate electrode 106 may be positively or negatively biased with respect to the source electrode 98 depending on the characteristics of the field-effect transistor 92.

Reference is now made to FIGURE 7 which is a perspective view, partially in cross section, of an integrated semiconductor device which includes two field-effect transistors having a common substrate. The integrated device comprises a body 140 of semiconductor material on which two gate electrodes 144 and 146 are formed. The gate electrodes 144 and 146 are insulated from the substrate by layers of grown silicon dioxide which overlie an inversion layer or conductive channel C connecting the source and drain regions *S* and *D* which are formed by diffusion of doped silicon dioxide as explained in connection with FIGURES 1 and 2 Deposited silicon dioxide overlies a portion of the diffused source and drain regions *S* and *D*, as also previously explained. The conductive electrodes 150 and 154 are the drain electrodes. A conductor 156 connects the drain electrode 150 to the source electrode 152, placing the source-to-drain current paths of the two field-effect transistors in series.

The device shown in FIGURE 7 may be encapsulated or packaged as a six terminal field-effect transistor suitable for use as the single active element of a cascode amplifier circuit similar to the one shown in FIGURE 6. The substrate of semiconductor material 140 is mounted on a conductive base or header 142. The base 142 may be connected to a point of fixed bias potential to maintain the substrate reverse direct current biased with respect to the operating potential of the source and drain electrodes. This connection provides the desired isolation between the output and input circuits of the amplifier and an alternating current signal reference to provide operation without signal distortion.

To operate the integrated device shown in FIGURE 7 in a cascode amplifier circuit, input signals are applied between the gate electrode 144 and the source electrode 148, which is grounded. Output signals are derived from the drain electrode 154. The gate electrode 146 is coupled to ground through a capacitor to provide for isolation between the drain and source electrodes 154 and 152 as previously explained. The header 142 is grounded, as shown in FIGURE 7, in order to d-c reverse bias the substrate 140 with respect to the potential of the drain electrodes 150 and 154 and the source electrode 152. An operating voltage is applied between the drain electrode 154 and the source electrode 148, and biasing circuit means are coupled to the gate electrodes 144 and 146 to determine the operating point of the integrated device. The reference characters *a, b, c, d, e* and *f* of FIGURES 6 and 7 indicate the electrodes of the devices shown in FIGURE 7 which correspond to the electrodes of transistors 90 and 92 shown in FIGURE 6.

Other versions of a field-effect transistor which may be used in practicing the invention are shown in FIGURES 8 and 9. FIGURE 8 shows an insulated gate field-effect transistor having a source electrode 160, a drain electrode 162, gate electrodes 164 and 166 and an intermediate electrode 168 which operates as a drain electrode with respect to the source electrode 160, and as a source electrode with respect to the drain electrode 162. The device shown in FIGURE 8 may be encapsulated to provide connections to the various electrodes including the common substrate 170 so that the device may be connected for operation as a cascode amplifier.

The source electrode 160 and the drain electrode 162 correspond respectively to the source electrode 148 and the drain electrode 154 of the device shown in FIGURE 7. Input signals are applied to the gate electrode 164. The electrode 168 is shown having a terminal so that the gate electrode 166 may be d-c referenced to the electrode 168 for zero-bias-voltage operation of the output stage. The electrodes of the device shown in FIGURE 8 have been identified by the source reference characters *a, b, c, d, e* and *f*, to show how the device of FIGURE 8 may be connected in a cascode amplifier circuit similar to the one shown in FIGURE 6.

FIGURE 9 shows an insulated gate field-effect transistor having two gate electrodes 172 and 174 controlling a single conductive channel *C*, which channel connects the source and

drain regions *S* and *D*. A source electrode 176 and a drain electrode 178 respectively correspond to the source and drain regions *S* and *D*.

The device shown in FIGURE 9 has a single substrate 180, so that a single ground connection is used for a cascode amplifier operation. Input signal energy may be applied to the gate electrode 172. The gate electrode 174 is biased to a potential intermediate that of the source and drain electrodes 176 and 178. When connected for operation in a cascode amplifier the device of FIGURE 9 may be considered as having a virtual intermediate electrode corresponding to the drain electrode of the input transistor portion and the source of the output transistor portions. Accordingly, the d-c bias at the gate electrode 174 may be considered as being referred to the virtual electrode.

The device shown in FIGURE 9 may also be connected in a cascode amplifier circuit similar to the circuit shown in FIGURE 6. The source, gate and drain electrodes of the device shown in FIGURE 9 are also identified by the reference characters *a*, *b*, *d*, *e* and *f* to illustrate how the device is connected in a cascode amplifier circuit similar to the circuit shown in FIGURE 6.

It should be noted that FIGURES 7, 8 and 9 are perspective views, partially in cross section, of insulated gate field-effect transistors which are not of a circular or concentric configuration as the configuration of the transistor shown in FIGURE 1. The source, gate and drain electrodes extend at an angle from the plane of the drawing, as shown. As previously explained, FIGURE 2 shows a transistor having a single drain electrode 24, a single gate electrode 22 and a single source electrode 16. In comparison the transistor shown in FIGURE 7 has two drain electrodes 150 and 154, two source electrodes 148 and 152, and two gate electrodes 144 and 146. Similarly, the field-effect transistors shown in FIGURES 8 and 9 are of a linear rather than circular configuration.

WHAT WE CLAIM IS:—

1. A signal translating circuit comprising: a field-effect semiconductor device with source, gate and drain electrodes formed on a substrate of semiconductor material, said gate electrode being insulated from said substrate, circuit means connecting said field-effect device as an active element of said signal translating circuit with one of said source, gate, and drain electrodes as an input electrode, a second one of said source, gate and drain electrodes as an output electrode, and the remaining one of said source, gate and drain electrodes as a common electrode; other circuit means providing a point of relatively fixed potential for said signal translating circuit referenced with respect to said common electrode, and means connecting said substrate to said point of fixed potential.

2. A signal translating circuit according to Claim 1 wherein said input electrode is one of said gate and source electrodes and said output electrode is said drain electrode.

3. A signal translating circuit according to Claim 1 wherein said circuit means include operating potential supply means and input, output and common terminals connected to said gate, source and drain electrodes, and means couple said substrate to said circuit means to maintain said substrate at substantially the potential of said common terminal for signal frequencies and to maintain a direct voltage difference between said substrate and said common terminal.

4. A signal translating circuit according to Claim 3 wherein said coupling means maintain said substrate at a direct voltage of a value to maintain said substrate reverse-biased relative to said source and drain electrodes.

5. A signal translating circuit according to Claim 3 or Claim 4 wherein said coupling means maintain a difference of zero volts direct voltage between said substrate and said common terminal.

6. A signal translating circuit according to any one of the preceding claims wherein said field-effect semiconductor device has a pair of rectifying junctions respectively coupled (a) between said substrate and one of said common and input electrodes and (b) between said substrate and said output electrode, and wherein said signal translating circuit is stabilized by further circuit means connecting said substrate and said common electrode to each other to isolate said input and output electrodes from each other.

7. A signal translating circuit according to Claim 3 or Claim 4 or Claim 5 wherein said circuit means provide a signal input circuit coupled between said source electrode and a point of reference potential and further provide a signal output circuit coupled between said drain electrode and said point of reference potential, and wherein said coupling means provide low impedance at signal frequencies and couple said gate electrode to said point of reference potential, and further couple said substrate electrode to said point of reference potential.

8. A signal translating circuit comprising: first and second field-effect transistors each having source and drain electrodes, said electrodes being formed on a single substrate of semiconductor material, each said transistor having a gate electrode insulated from said substrate, and said source and drain electrodes of said first and second field-effect transistors each being effectively coupled to said substrate by a rectifying junction poled so that a positive potential applied to said substrate with respect to the potential of the corresponding one of said source and drain elec-

drain regions *S* and *D*. A source electrode 176 and a drain electrode 178 respectively correspond to the source and drain regions *S* and *D*.

The device shown in FIGURE 9 has a single substrate 180, so that a single ground connection is used for a cascode amplifier operation. Input signal energy may be applied to the gate electrode 172. The gate electrode 174 is biased to a potential intermediate that of the source and drain electrodes 176 and 178. When connected for operation in a cascode amplifier the device of FIGURE 9 may be considered as having a virtual intermediate electrode corresponding to the drain electrode of the input transistor portion and the source of the output transistor portions. Accordingly, the d-c bias at the gate electrode 174 may be considered as being referred to the virtual electrode.

The device shown in FIGURE 9 may also be connected in a cascode amplifier circuit similar to the circuit shown in FIGURE 6. The source, gate and drain electrodes of the device shown in FIGURE 9 are also identified by the reference characters *a*, *b*, *d*, *e* and *f* to illustrate how the device is connected in a cascode amplifier circuit similar to the circuit shown in FIGURE 6.

It should be noted that FIGURES 7, 8 and 9 are perspective views, partially in cross section, of insulated gate field-effect transistors which are not of a circular or concentric configuration as the configuration of the transistor shown in FIGURE 1. The source, gate and drain electrodes extend at an angle from the plane of the drawing, as shown. As previously explained, FIGURE 2 shows a transistor having a single drain electrode 24, a single gate electrode 22 and a single source electrode 16. In comparison the transistor shown in FIGURE 7 has two drain electrodes 150 and 154, two source electrodes 148 and 152, and two gate electrodes 144 and 146. Similarly, the field-effect transistors shown in FIGURES 8 and 9 are of a linear rather than circular configuration.

WHAT WE CLAIM IS:—

1. A signal translating circuit comprising: a field-effect semiconductor device with source, gate and drain electrodes formed on a substrate of semiconductor material, said gate electrode being insulated from said substrate, circuit means connecting said field-effect device as an active element of said signal translating circuit with one of said source, gate, and drain electrodes as an input electrode, a second one of said source, gate and drain electrodes as an output electrode, and the remaining one of said source, gate and drain electrodes as a common electrode; other circuit means providing a point of relatively fixed potential for said signal translating circuit referenced with respect to said common electrode, and means connecting said substrate to said point of fixed potential.

2. A signal translating circuit according to Claim 1 wherein said input electrode is one of said gate and source electrodes and said output electrode is said drain electrode.

3. A signal translating circuit according to Claim 1 wherein said circuit means include operating potential supply means and input, output and common terminals connected to said gate, source and drain electrodes, and means couple said substrate to said circuit means to maintain said substrate at substantially the potential of said common terminal for signal frequencies and to maintain a direct voltage difference between said substrate and said common terminal.

4. A signal translating circuit according to Claim 3 wherein said coupling means maintain said substrate at a direct voltage of a value to maintain said substrate reverse-biased relative to said source and drain electrodes.

5. A signal translating circuit according to Claim 3 or Claim 4 wherein said coupling means maintain a difference of zero volts direct voltage between said substrate and said common terminal.

6. A signal translating circuit according to any one of the preceding claims wherein said field-effect semiconductor device has a pair of rectifying junctions respectively coupled (a) between said substrate and one of said common and input electrodes and (b) between said substrate and said output electrode, and wherein said signal translating circuit is stabilized by further circuit means connecting said substrate and said common electrode to each other to isolate said input and output electrodes from each other.

7. A signal translating circuit according to Claim 3 or Claim 4 or Claim 5 wherein said circuit means provide a signal input circuit coupled between said source electrode and a point of reference potential and further provide a signal output circuit coupled between said drain electrode and said point of reference potential, and wherein said coupling means provide low impedance at signal frequencies and couple said gate electrode to said point of reference potential, and further couple said substrate electrode to said point of reference potential.

8. A signal translating circuit comprising: first and second field-effect transistors each having source and drain electrodes, said electrodes being formed on a single substrate of semiconductor material, each said transistor having a gate electrode insulated from said substrate, and said source and drain electrodes of said first and second field-effect transistors each being effectively coupled to said substrate by a rectifying junction poled so that a positive potential applied to said substrate with respect to the potential of the corresponding one of said source and drain elec-

* C L M S *

trodes renders said rectifying junction conductive; means connecting the source-to-drain current paths of said first and second field-effect transistors in series; means for applying a bias potential across the series combination of said source-to-drain current paths of said first and second field-effect transistors; circuit means for biasing said gate electrodes to predetermined bias potentials; capacitative means coupling the gate electrode of said first field-effect transistor to the source electrode of said second field-effect transistor to provide an alternating current point of reference potential to said gate electrode of said first field-effect transistor; input circuit means coupled between the gate and source electrodes of said second field-effect transistor for applying input signals to said amplifier circuit; output circuit means coupled to the drain electrode of said first field-effect transistor for deriving output signals, and means coupling said substrate to said source electrode of said second field-effect transistor to prevent energy from feeding back from said output circuit to said input circuit.

9. A signal translating circuit according to Claim 1 wherein said field-effect semiconductor device has first, second and third electrodes formed on a substrate of semiconductor material and two gate electrodes insulated from said substrate, said first, second and third electrodes being effectively coupled to said substrate by a rectifying junction poled so that a positive potential applied to said substrate with respect to the potential of the corresponding one of said first, second and third electrodes renders said rectifying junctions conductive, said second electrode effectively operating as the source and drain electrodes with respect to said first and third electrodes respectively; a resistor is coupled between said second electrode and one of said gate electrodes; circuit means are provided for forward biasing said other gate electrode with respect to said third electrode; a capacitor couples said one gate electrode to a point of reference potential; means are coupled between the other gate electrode and said point of reference potential for applying an input signal; circuit means are coupled between said first electrode and said point of reference potential for deriving an output signal; and means couple said third electrode and said substrate to said point of reference potential to prevent energy from being fed back from said first electrode to said second electrode.

10. A signal translating circuit according to Claim 1 wherein there are: first and second field-effect transistors each having source and drain electrodes formed on a substrate of semiconductor material and a gate electrode insulated from said substrate; means connecting the source-to-drain current paths of said first and second field-effect transistors in series; circuit means providing a signal input circuit coupled between the gate and source electrodes of said first field-effect transistor; other circuit means providing an output circuit coupled between said drain electrode of said second field-effect transistor and said source electrode of said first field-effect transistor; further circuit means providing a low impedance at signal frequencies coupling said gate electrode of said second field-effect transistor and said source electrode of said first field-effect transistor; and means providing a low impedance at said signal frequencies coupling said substrate of said first and second field-effect transistors to said source of said first field-effect transistor to prevent energy from feeding back from said signal output circuit to said signal input circuit.

11. A signal translating circuit according to Claim 1 wherein there are: first and second field-effect transistors each having source and drain electrodes formed on a substrate of semiconductor material and a gate electrode insulated from said substrate; circuit means including operating potential supply means, and input, output and common terminals connected to said gate, source and drain electrodes of said first and second field-effect transistors so that said first and second field-effect transistors operate as the active devices in said signal translating circuit; and means coupling said substrate to said circuit means to maintain said substrate at substantially the potential of said common terminal for signal frequencies and at a direct voltage of a value to maintain said substrate reverse biased relative to said source and drain electrodes.

12. A signal translating circuit according to Claim 1 wherein said signal translating circuit is in the form of a cascode amplifier circuit and the field-effect device is a transistor having two gate electrodes insulated from said substrate, and wherein means including operating potential supply means are connected between said drain and source electrodes; signal input circuit means are coupled between one of said gate electrodes and said source electrode; signal output circuit means are coupled between said source and drain electrodes; and means connect said substrate to said source electrode so as to isolate said signal input circuit from said signal output circuits.

13. A signal translating circuit according to Claim 1 wherein said field-effect semiconductor device has two gate electrodes insulated from said substrate; means are provided for applying an operating potential between said source and drain electrodes; circuit means are provided for biasing said gate electrodes to predetermined bias potentials; capacitive means couple one of said gate electrodes to said source electrode to prevent energy feedback from said drain electrode to said one

gate electrode; means are coupled between the other gate electrode and said source electrode for applying input signals; circuit means are coupled between said drain and source electrodes for deriving output signals; and means couple said substrate to said source electrode to prevent energy from feeding back from said output circuit to said input circuit.

14. A signal translating circuit substantially as herein described with respect to FIGURE 5 of the accompanying drawings.

15. A signal translating circuit substantially as herein described with respect to FIGURE 6 of the accompanying drawings.

16. A signal translating circuit substantially as herein described with respect to FIGURE 7 of the accompanying drawings.

17. A signal translating circuit substantially as herein described with respect to FIGURE 8 of the accompanying drawings.

18. A signal translating circuit substantially as herein described with respect to FIGURE 9 of the accompanying drawings.

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