

ABSTRACT

A memory system according to an embodiment includes: a first chip including a first plane and a first input/output circuit; and a controller which is capable of issuing a
5 command for controlling the first chip. The first plane includes: a first memory cell array having a plurality of first memory cell transistors; and a first latch circuit which is capable of storing first read data read from the first memory cell array. The first input/output circuit
10 includes a first FIFO circuit which is capable of fetching the first read data from the first latch circuit. The controller is capable of transmitting to the first chip a first command for ordering fetching of the first read data from the first latch circuit to the first FIFO circuit
15 during a period in which a read operation is executed on the first plane.