Improve Transistor Mobility by Adjusting Stress in Shallow Trench Isolation

ABSTRACT OF THE DISCLOSURE

A method of improving transistor carrier mobility by adjusting stress through recessing shallow trench isolation is presented. A trench is formed in a substrate. The trench is filled with a dielectric. A CMOS transistor is formed adjacent to the trench. A silicide layer is formed on the source/drain region. A recess is formed by etching the dielectric so that the surface of the dielectric is substantially lower than the surface of the substrate. Recessing the STI removes the compressive stress applied to the channel region by the STI material. A contact etch stop layer (CESL) is formed over the gate electrode, spacers, source/drain regions and the dielectric. The CESL applies a desired stress to the channel region. Trench liners are optionally formed to provide a stress to the channel region. A spacer can optionally be formed in the STI recess.

Fig. 7