

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
11 July 2002 (11.07.2002)

PCT

(10) International Publication Number
WO 02/054371 A1

(51) International Patent Classification⁷: **G09B 23/18**

(21) International Application Number: PCT/SG01/00021

(22) International Filing Date: 2 January 2001 (02.01.2001)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant (for all designated States except US): **AD-DEST TECHNOVATION PTE. LTD.** [SG/SG]; 101 Cecil Street, #09-07 Tong Eng Building, Singapore 069533 (SG).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **GOH, Zenton** [SG/SG]; Blk 642, Choa Chu Kang Street 64, #08-77, Singapore 680642 (SG). **LIM, Soh, Min** [SG/SG]; Blk

309, Canberra Road, #16-109, Singapore 750309 (SG). **NEO, Sian, Sheng** [SG/SG]; 50 Choa Chu Kang North 7, #03-09, Singapore 689527 (SG). **TAN, Kah, Chye** [SG/SG]; 16 Amber Gardens, #17-03, Singapore 439961 (SG).

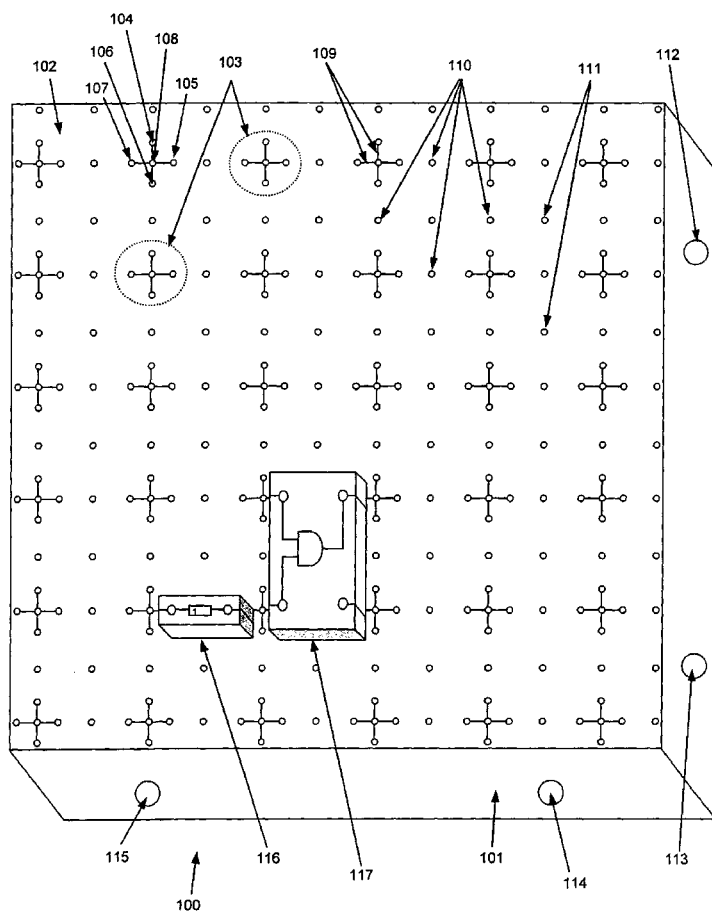
(74) Agents: **NAMAZIE, Farah** et al.; Haq & Namazie Partnership, Robinson Road, P.O. Box 765, Singapore 901515 (SG).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian

[Continued on next page]

(54) Title: BREADBOARD USED FOR EDUCATIONAL PURPOSES



(57) Abstract: A breadboard for building and displaying electronic circuits used for educational purposes comprises a panel housing, an assembly panel attached to and covering the panel housing, a plurality of contact stations located on and periodically distributed over the assembly panel such that they form a regular grid, which contact stations are electrically isolated from each other and capable of receiving electronic component blocks, a plurality of first power supply points located on and periodically distributed over the assembly panel such that they form a regular grid, which first power supply points are electrically connected to each other, and a plurality of second power supply points located on and periodically distributed over the assembly panel such that they form a regular grid, which second power supply points are electrically isolated from the first power supply points, wherein the grids formed by the contact stations, the first power supply points and the second power supply points have the same periodicity.

WO 02/054371 A1



patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

— *with international search report*