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## (54) IMPROVEMENTS IN OR RELATING TO APPARATUS FOR RECORDING CHARACTERS OR SYMBOLS IN DOT MATRIX FORM

(71) We, KABUSHIKI KAISHA SEIKOSHA, a Japanese company of 5, 2-chome, Kyobashi, Chuo-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

5 This invention relates to apparatus for recording letters, numerals or other symbols or characters in dot matrix form. The principal object of the invention is to provide an apparatus which will record a character or symbol with a desired magnification in the row and/or column direction of the matrix in such manner that, despite such magnification, the character or symbol recorded is clear and recognisable. 5

10 In general, if a letter, a numeral or other character or symbol is formed by a dot matrix, consisting of dots and non-dots, i.e. blanks and the character or symbol does not exceed a certain size, it is usually clear and recognisable enough to be read and understood easily but when such a dot character is enlarged beyond such certain size range, it becomes, in many cases, difficult to read and understand. For example, in the case of letters such as 'E' and 'F' 15 composed entirely of horizontal and vertical lines their clearness is not greatly lessened even after considerable enlargement. On the other hand with letters such as 'R' and 'X' containing oblique or curved lines clarity is lost upon enlargement and reading and understanding become difficult. Figure 1 of the accompanying drawings shows an example of an enlarged 'R', i.e. it shows an original dot pattern as shown in the accompanying Figure 2 which has 20 been enlarged by a magnification of 2 in the longitudinal or vertical direction (the column direction in the matrix) and also by the same magnification in the lateral direction (the row direction of the matrix). A comparison of Figures 1 and 2 shows how much less clear and recognisable as an 'R' is the letter in Figure 1 compared with that of Figure 2. 20

It is known to improve the clarity of characters formed by dots and including oblique lines by adding extra dots for 'compensation' between enlarged dots. In this known prior practice, however, the size of the character is standardized and there is no 'compensation' 25 provided in the vertical and horizontal directions.

The present invention seeks to overcome the foregoing difficulties and provide improved apparatus for recording a character or symbol from a pattern of separate display picture elements or 'dots'. 30

According to a feature of this invention, there is provided an apparatus for magnifying an original letter, numeral or other symbol or character in dot matrix form comprising:- storage means for storing a bit pattern in which dots forming said character or symbol and non-dots (blanks) are converted into bits of a first logic value and into bits of a second logic value respectively; matrix row magnification setting means and matrix column 35 magnification setting means for setting desired row and column magnifications respectively of the character or symbol to be recorded; first means for reading out the bits which constitute data stored in said storage means; selecting means for selecting the respective bits in accordance with a predetermined order; first magnification converting means for forming bits each of which has the same logic value as the selected bit and the number of which is 40 equal to that set in said matrix row magnification setting means; second magnification converting means for forming bits each of which has the same logic value as the selected bit and the number of which is equal to that set in said matrix column magnification setting means; and second means for recording a magnified dot symbol or character in accordance 45 with the respective bits formed by said first and second magnification converting means. 45

According to another feature of the invention there is provided an apparatus for magnifying and clarifying an original letter, numeral or other symbol or character in dot matrix form comprising:— storage means for storing a bit pattern in which dots forming said character or symbol and non-dots (blanks) are converted into bits of a first logic value and of a second logic value respectively; matrix row magnification setting means and matrix column magnification setting means for setting desired row and column magnifications respectively of the character or symbol to be recorded; first means for reading out the bits which constitute data stored in said storage means; selecting means for selecting the respective bits in accordance with a predetermined order; detecting means for detecting whether or not the array of a bit having the second logic value selected by said selecting means and surrounding bits thereof coincides with a predetermined rule and, if such coincidence is detected, converting the selected bit into a bit having the first logic value; first magnification converting means for forming bits each of which has the first logic value when the selected bit coincides with the first logic value or with the second logic value to be converted by said detecting means and has the second logic value when the selected bit is not converted by said detecting means and the number of which coincides with that set in said matrix row magnification setting means; second magnification converting means for forming bits each of which has the first logic value when the selected bit coincides with the first logic value or with the second logic value to be converted by said detecting means and has the second logic value when the selected bit is not converted by said detecting means and the number of which coincides with that set in said matrix column magnification setting means; and second means for recording a magnified dot symbol or character in accordance with the respective bits formed by said first and second magnification converting means.

The detecting means may comprise:— means for detecting whether there is satisfaction of the condition that in the aforesaid bit pattern two bits of said first logic value adjoin in an oblique direction and that each of two bits of said second logic value adjoins each of the aforementioned two bits of the first logic value; and means for converting one of said two bits of the second logic value into one bit of the first logic value if satisfaction of said condition is detected.

The detecting means may comprise:— means for detecting whether there is satisfaction of the condition that in an arbitrary three bits of said first logic value, the first, second and third bits are formed in an oblique direction, and that two other bits of said first logic value are formed in a row or in a column direction such that one bit of said two other bits adjoins said first bit and the other bit of said two other bits adjoins said one bit, and that the angle between the aforementioned oblique and row or column directions is within 90°; and means for converting one bit of the second logic value which adjoins said first and second bits into a bit of the first logic value if satisfaction of said condition is detected.

As will be understood more clearly later, in carrying out the invention a character or symbol is recorded in a matrix pattern which is composed of a plurality of picture elements or 'dots' and 'non-dots' (i.e. blanks) and the magnifications in a longitudinal (matrix column) and a lateral (matrix row) directions of the said pattern can be set to any desired value to form a character with a desired enlargement whereby characters or symbols of a wide variety of forms and in any of a wide range of desired sizes can be formed. Also, when effecting enlargement of a character, dot interpolation can be performed in accordance with empirically found rules by adding interpolated dots which maintain the clarity and recognisability of the symbol or character, so that, despite possibly considerable enlargement, it remains easy to read.

One object of the invention is, therefore, to form a character of a desired size by enlarging a character formed by a pattern of picture elements in desired magnification in both the longitudinal and lateral directions. As will be seen later, the magnifications in these two mutually perpendicular directions do not have to be the same.

A second object of the invention is to subject an enlarged character formed by a pattern of picture elements to interpolation by dot additions in accordance with empirically found rules, so that no matter to what extent enlargement of the character or symbol takes place, the enlarged character or symbol is clearly recognisable.

As will be seen later, the invention provides apparatus which will achieve the foregoing objects and nevertheless be a self-contained single apparatus of relatively small size which does not require, for its operation, a separate external system such as a computer.

The invention is illustrated in and explained in connection with the accompanying drawings, in which:—

Figures 1 to 7 are explanatory dot matrix figures which are used to explain the methods of dot interpolation carried out by apparatus which is in accordance with an embodiment of the invention and is illustrated in later figures;

Figures 8 to 19 inclusive are logic circuit diagrams illustrating apparatus in accordance with embodiments of the invention;

Figure 20 is a bit pattern or table which expresses the dot pattern of Figure 2;

Figures 21 and 22 are bit content tables illustrating storage conditions of the registers  $M_1$  to  $M_5$  shown in preceding figures;

Figure 23 shows the letter 'R' formed from a dot matrix and as it would appear enlarged by an embodiment of the invention;

Figure 24 is a bit table showing an example of interpolation carried out in accordance with an embodiment of this invention; and

Figures 25 and 26 show parts of bit tables and also serve to illustrate interpolation methods in accordance with an embodiment of the invention.

Before proceeding to describe embodiments of the present invention, the term 'interpolation' as herein used will first be explained. This term 'interpolation' as herein employed, means the provision, in a dot matrix pattern of a plurality of additional dots between adjacent dots properly belonging to said pattern, in order to make the character or other symbol represented by the interpolated pattern more clearly recognisable than it was before interpolation i.e. before the additional dots were added.

Figure 2 shows the letter R formed by dots in a dot matrix of 7 rows and 5 columns. Figure 3 shows the letter R as it appears after enlargement by doubling the number of rows and trebling the number of columns. The result is a letter the recognisability of which has been impoverished as a result of enlargement. In order to understand how such loss of clarity can be avoided by interpolation, consider the original dot pattern of Figure 2 to be divided into areas in 7 rows and 5 columns as shown by the broken lines in Figure 2. Some of the areas have a dot and some are blank. Now consider any area  $n, m$  (where  $n$  is the number of the row and  $m$  is the number of the column) and assume a small matrix of 3 rows and 3 columns including the area  $n, m$  to be formed, said small matrix being picked out from Figure 2 so that, the area  $n, m$  is in the position  $(p, q)$  in the small matrix where  $p$  is the number of the row and  $q$  is the number of the column in the small matrix, the sum of  $p$  plus  $q$  is an odd number. If, in such a small matrix, the dot pattern is as shown in any of the small matrices represented at A to H inclusive of Figure 4, interpolation is effected in a portion  $d$  of a blank area  $a_{n,m}$  between dotted areas  $b_1$  and  $b_2$ . Applying this to Figure 2, it will be seen that the area  $(5, 2)$  which corresponds with a number of enlarged areas, including the enlarged area  $(9, 6)$  of Figure 3, is interpolated and a dot  $d_0$  shown by a broken line circle in Figure 3 is formed where indicated.

In this way, each area  $n, m$  in Figure 2 is considered a matrix of 3 rows and 3 columns and decision is made whether interpolation is needed or not.

The clearness of a character is substantially improved by the foregoing first interpolation method. However still better clarity can be obtained by a second interpolation method which will now be described. In this method each blank area  $(p, q)$  is considered and a small matrix of 2 rows and 2 columns including said blank area  $(p, q)$  is assumed. If any one blank area  $a_{n,m}$  is considered ( $n$  and  $m$  being the row and column numbers respectively of the blank area) the two rows and columns of the small matrix will be  $(a_{n-1, m} \ a_{n-1, m+1})$ .

If, in such small matrix, the area  $a_{n-1, m+1}$  corresponding to the blank area  $a_{n,m}$  is blank, and the areas  $a_{n-1, m}$  and  $a_{n, m+1}$  are dotted (as in the case in Figure 5c) interpolation is performed in part of the blank area  $a_{n,m}$ .

A to D of Figure 5 show all positional relationships between blank areas  $C_1$  to  $C_4$  and dotted areas  $b_1$  and  $b_2$ , and also show interpolation in each case in the same manner as in Figure 4 i.e. by diagonal lines. If this second interpolation method is applied to Figure 2, interpolation is performed at  $(1, 5)$ ,  $(2, 4)$ ,  $(3, 4)$ ,  $(4, 5)$ ,  $(5, 4)$ ,  $(6, 3)$ ,  $(7, 4)$  and  $(6, 5)$  of Figure 2. In this way areas to be interpolated are decided.

Explanation will now be given on the rules for forming dots in the areas to be interpolated when the original matrix character is enlarged. Figure 6 shows the case in which an original small matrix pattern as illustrated in Figure 5C is enlarged to  $S$  times the number of columns and  $T$  times the number of rows. In Figure 6, the portion of this small matrix to be interpolated is the portion H. Figure 7 shows at D the case in which the interpolation portion H alone has been picked up. In the same way Figure 5 shows enlarged, at A to C respectively the areas requiring interpolation and the results obtained on such enlargement. In Figure 7 the references 'o' to 'x' inclusive represent the number of columns in each area of the small matrix, and the references 'o' to 'y' inclusive indicate the number of rows. The position and number of dots at which interpolation takes place is decided so as to satisfy the following expressions:

In Figure 7A,

$$Tx + Sy \geq ST \dots (1)$$

In Figure 7B,

$$T(x+1) + S(y+1) \geq ST \dots (2)$$

In Figure 7C,

$$Sy \geq T(x+1) \dots (3)$$

In Figure 7D,

$$S(y+1) \leq Tx \dots (4)$$

The above expressions of inequalities indicate the number of dots to be formed in the areas requiring interpolation, and have been derived experimentally as satisfying the requirement of ensuring that the enlarged interpolated character or symbol retains good recognisability.

Having described methods of enlarging a character or symbol and interpolating to retain recognisability and clarity there will now be described, with reference to Figures 8 to 17 inclusive, an embodiment of the invention for carrying out those methods. Referring to Figure 8 K is a keyboard composed of switch keys each appropriate to a different letter, symbol or the like. Data information selected by operation of these keys is transferred to registers R<sub>1</sub> and R<sub>2</sub> by means of a data multiplexer D. The registers R<sub>1</sub> and R<sub>2</sub> are magnification registers. A third register R<sub>3</sub> stores data such as a letter, or other symbol of which one word is read out and written in a storage latch R<sub>4</sub>. An arithmetic unit AD shown in Figure 10 performs addition and subtraction between various count contents and stored contents and specific operational outputs from said arithmetic unit AD is stored in a storage latch R<sub>5</sub>. A storage latch R<sub>6</sub> shown in Figure 11 temporarily stores the output of a counter C<sub>4</sub>. A shift register R<sub>7</sub> shown in Figure 17, having a capacity of 7 bits, stores dot data for recording. A character generator CG shown in Figure 12 effects code conversion of the output data of the storage latch R<sub>4</sub> shown in Figure 8. This output is stored by shift registers M<sub>1</sub> to M<sub>9</sub> shown in Figure 12. These shift registers M<sub>1</sub> to M<sub>9</sub> have the function of shifting in both the vertical and the horizontal directions in the drawing. An interpolation detecting unit U is used to detect whether interpolation is required or not on the basis of the bit pattern of the original character. The details of this circuit are shown in Figure 16. This circuit is arranged to take out each output of the bit pattern stored in the registers M<sub>1</sub> to M<sub>9</sub> and logically detect the need for the first and second interpolations. A storage latch R<sub>8</sub> shown in Figure 15 stores specific operational outputs b<sub>1</sub> to b<sub>4</sub> of the arithmetic unit AD illustrated in Figure 10.

In Figure 11 C<sub>1</sub> is a heptal (seven counting) counter and C<sub>2</sub> indicates a preset counter in which '7' is set. P<sub>1</sub> is a coincidence circuit, C<sub>3</sub> and C<sub>4</sub> are binary counters and P<sub>2</sub> is a comparison circuit. C<sub>5</sub> in Figure 12 is a pental (five counting) timing counter and produces timing pulses at terminals d<sub>1</sub> to d<sub>5</sub>. '5' is set in a pre-set counter C<sub>7</sub> shown in Figure 13 and when counter C<sub>6</sub> counts '5', an output is produced from coincidence circuit P<sub>3</sub>. Counter C<sub>8</sub> shown in Figure 14 has a decimal counting function. '9' is set in a pre-set counter, C<sub>9</sub> and upon coincidences with the output of the counter C<sub>8</sub>, an output is produced from coincidence circuit P<sub>4</sub>. A decoder DC shown in Figure 15 produces an output when the magnification of a character is '1', '7', '14' ... P<sub>5</sub> is a coincidence circuit. Monostable multivibrators N<sub>1</sub> to N<sub>10</sub> shown in Figures 9 and 12 to 15 are used for providing output timing and also for waveform shaping.

DL shown in Figure 11 is a delay circuit and F<sub>1</sub> and F<sub>2</sub> shown in Figure 14 are R-S flip-flop circuits. DR shown in Figure 17 is a driving device for operating a wire dot printer and, in the particular embodiment now being described it is assumed that dots are formed by moving 7 pins (PN) in the lateral direction. In Figure 17, AC<sub>1</sub>, AC<sub>2</sub> and AC<sub>3</sub> are multipliers; B<sub>1</sub>, B<sub>2</sub>, B<sub>3</sub> and B<sub>4</sub> are adders; and P<sub>6</sub> to P<sub>9</sub> are coincidence circuits. In Figures 8 to 17, G<sub>1</sub> to G<sub>137</sub> and G<sub>197</sub> to G<sub>198</sub> are gate circuits.

Detailed explanation of the interpolation detecting circuit U shown in Figure 16 will now be given below. The values in the storage sections 1A to 1E inclusive to 9A to 9E inclusive of the registers M<sub>1</sub> to M<sub>9</sub> shown in Figure 12 are fed to the input terminals of the gates indicated by the corresponding references in Figure 16. Figure 16 illustrates logic circuitry which effects both the first and second interpolations previously mentioned and the detailed explanation of which are given below.

First, in the first interpolation method, if the matrix of 3 rows and 3 columns is

$$\begin{matrix} B_{p,q} & B_{p,q+1} & B_{p,q+2} \\ B_{p+1,q} & B_{p+1,q+1} & B_{p+1,q+2} \\ B_{p+2,q} & B_{p+2,q+1} & B_{p+2,q+2} \end{matrix}$$

and the bit regarded is bp+1,q, then, when the relationship

$$\frac{B_{p+1,q} \cdot B_{p+1,q+2} \cdot B_{p,q+2} \cdot B_{p+1,q+1} \cdot B_{p+2,q+2}}{(B_{p+2,q+1} \cdot B_{p+2,q} + B_{p,q} \cdot B_{p,q+1}) \times (B_{p+2,q} \cdot B_{p+2,q+1} + B_{p,q} \cdot B_{p,q+1})} = 1 \dots (5)$$

is satisfied, the bit  $B_{p+1, q}$  is converted to '1'.

If the bit regarded is  $B_{p, q+1}$ , then when the relationship

$$\frac{B_{p, q+1}}{(B_{p, q} \cdot B_{p+1, q} + B_{p, q+2} \cdot B_{p+1, q+2})} \times (B_{p, q} \cdot B_{p+1, q} + B_{p, q+2} \cdot B_{p+1, q+2}) = 1 \dots (6)$$

is satisfied this bit is converted to '1'. Similarly if the bit regarded is  $B_{p+1, q+2}$  then when the relationship

$$\frac{B_{p+1, q+2}}{(B_{p, q+1} \cdot B_{p+2, q+1} + B_{p+1, q+3} \cdot B_{p+2, q+3})} \times (B_{p, q+1} \cdot B_{p+2, q+1} + B_{p+1, q+3} \cdot B_{p+2, q+3}) = 1 \dots (7)$$

is satisfied, this bit is converted to '1'; and if  $B_{p+2, q+1}$  is the bit regarded, this bit is converted to '1' if the relationship

$$\frac{B_{p+2, q+1}}{(B_{p+1, q} \cdot B_{p+2, q} + B_{p+1, q+2} \cdot B_{p+2, q+2})} \times (B_{p+1, q} \cdot B_{p+2, q} + B_{p+1, q+2} \cdot B_{p+2, q+2}) = 1 \dots (8)$$

is satisfied.

Now, if the matrix of 2 rows and 2 columns is

$$\begin{pmatrix} A_{p, q} & A_{p, q+1} \\ A_{p+1, q} & A_{p+1, q+1} \end{pmatrix}$$

and the bit regarded is  $A_{p+1, q}$  or  $A_{p, q+1}$ , then, when the relationship

$\frac{A_{p+1, q}}{(A_{p, q} \cdot A_{p+1, q} + A_{p, q+1} \cdot A_{p+1, q+1})} \times (A_{p, q} \cdot A_{p+1, q} + A_{p, q+1} \cdot A_{p+1, q+1}) = 1$  is satisfied, the bit  $A_{p+1, q}$  or  $A_{p, q+1}$  is converted to '1'. Similarly if the bit regarded is  $A_{p, q}$  or  $A_{p+1, q+1}$ , this bit is converted to '1' if the relationship

$\frac{A_{p, q}}{(A_{p, q} \cdot A_{p+1, q} + A_{p, q+1} \cdot A_{p+1, q+1})} \times (A_{p, q} \cdot A_{p+1, q} + A_{p, q+1} \cdot A_{p+1, q+1}) = 1$  is satisfied. Consequently, when the bit regarded is '0' and the relationship

$$\frac{A_{p+1, q}}{(A_{p, q} \cdot A_{p+1, q} + A_{p, q+1} \cdot A_{p+1, q+1})} \times (A_{p, q} \cdot A_{p+1, q} + A_{p, q+1} \cdot A_{p+1, q+1}) = 1 \dots (9)$$

is satisfied, the said bit is converted to '1'. Figure 16 illustrates the case in which the bit regarded was taken to be in the storage section 3C of the register  $M_3$  in Figure 12 and the logic relationships, set out above in expressions (5) to (9) above were satisfied.

An explanation will now be given of the operations which take place when an original dot pattern of the letter 'R' shown in Figure 2 is subjected to double enlargement as regards rows and treble enlargement as regards columns (as shown in Figure 3) and interpolation is performed. In Figure 8, the magnifications of '2' and '3' (for rows and columns respectively) of the character R, as well as the character data for one line of printing are set up in the keyboard K by selective operation of the appropriate keys and are written respectively into the magnification registers  $R_1$  and  $R_2$  and the data register  $R_3$  through the data multiplexer D. A printing instruction PSo given from the keyboard side is fed in as indicated by this reference and causes the letter 'R' to be read out from the register  $R_3$  and transcribed in the storage latch  $R_4$  for one word. The output Do from the storage latch is fed to the input of a character generator CG shown in Figure 12, where it is converted to a bit pattern as illustrated in Figure 20 in which the dots and blank areas shown in Figure 2 have been converted to '1' and '0' respectively. At the same time, the output PSo triggers the monostable multi-vibrator  $N_3$  through the gate circuit  $G_{65}$  shown in Figure 12. The output  $PS_1$  from  $N_3$  causes a logic (1,1) to be fed through the gate circuits  $G_{13}$  to  $G_{15}$  to two inputs of the arithmetic unit AD (Figure 10). The other two inputs of the arithmetic unit AD, that is, the outputs of the gate circuits  $G_{16}$  and  $G_{17}$ , are in the state (00), so that in one input of the arithmetic unit AD is fed (0011), that is, a decimal '3'. Also, the output at  $PS_1$  opens the gate circuits  $G_{26}$  to  $G_{29}$  shown in Figure 10 and the (0000) provided by the outputs  $a_1$  to  $a_4$  of the already-cleared counter  $C_6$  (Figure 13) is fed to the arithmetic unit AD. Consequently, '3' is produced in the output of said arithmetic unit AD, and the output  $PS_1$  of the multi-vibrator  $N_3$  (Figure 12) which has been triggered by the output PSo, goes to  $PS_2$  through the gate circuit  $G_{66}$ , so that '3' is written in the storage latch  $R_5$  (Figure 10). The outputs  $e_1$  to  $e_3$  of the storage latch  $R_5$  designate the third column of the character generator CG shown in Figure 12. Consequently, the data of the third column of the bit pattern shown

in Figure 20 is put out. The reason why the third column of the bit pattern of the letter 'R' is first read, is as follows. In both the foregoing first and second interpolation methods, regard is paid to a particular blank area and when the presence and absence of surrounding dots satisfy a pre-determined relationship, interpolation is performed to the said blank area. In this example, in which the presence and absence of dots correspond to logic '1' and '0' respectively, the regarded bit shifts to a certain storage section in the register and decision is made by the interpolation detecting circuit U as to whether the bit in such storage position is '1' or '0' and, when it is '0', as to whether the surrounding bit pattern requires the first or second interpolation method. Figures 25 and 26 show the case in which the foregoing dot patterns for interpolation have been converted to bit patterns of '1' and '0' and in which the bit  $b_0$  indicates a bit regarded. The data bits in each column of the bit pattern read from the character generator CG are stored in the registers  $M_3$  to  $M_9$ . In this example, the regarded bit is shifted to the storage section 3C of the register  $M_3$  and, with this bit as the centre, correlation thereof with surrounding bits is studied.

The third column of the bit pattern of Figure 20 stored in the character generator CG is designated by the outputs  $e_1$  to  $e_3$  of the storage latch shown in Figure 10 and the data bits of the third column (1001100) are fed to the registers  $M_3$  to  $M_9$  inclusive through the gate circuits  $G_{56}$  to  $G_{62}$  inclusive shown in Figure 12. The counter  $C_5$  is advanced by '1' by the foregoing output  $PS_2$ , thus producing an output at its terminal  $d_1$ , causing the contents of the registers  $M_1$  to  $M_9$  to be shifted by one bit to the right through the gate circuits  $G_{68}$  and  $G_{67}$ . As a result, the data bits of the third column mentioned above are transcribed in the storage sections 3A to 9A of the registers  $M_3$  to  $M_9$ . There are two registers  $M_1$  and  $M_2$  provided because at most, two bits in the two rows above the regarded bit are required as objects of detection.

Monostable multivibrator  $N_4$  is triggered by the output from terminal  $d_1$  and its output  $PS_3$  is fed to one input of the arithmetic unit AD through the gate circuits  $G_{13}$  to  $G_{17}$  inclusive (Figure 10). The outputs  $PS_3$  opens the gate circuit  $G_{30}$  through  $G_{33}$  and feeds the (0011) logic signals from the outputs  $e_1$  to  $e_4$  i.e. a decimal '3', to the other input of the arithmetic unit AD, so that (0010), i.e. decimal '2', is produced at the output of the arithmetic unit AD. This is written into the storage latch  $R_5$  when the output  $PS_2$  ceases. The data bits of the second column in the bit pattern of 'R' (see Figure 20) are designated by the outputs  $e_1$  to  $e_4$  of the storage latch  $R_5$  and are fed to the registers  $M_3$  to  $M_9$ . The counter  $C_5$  of Figure 12 is advanced by '1' by the foregoing output  $PS_2$  and counts '2'. The output at the terminal  $d_2$  causes the contents of the registers  $M_3$  to  $M_9$  to be shifted by one bit to the right and the data bits of the third column are transcribed in the storage sections 3B to 9B and the data bits of the second column are put in the storage sections 3A to 9A. In the same way, the data bits of the first column are transcribed in the storage sections 3A to 9A of the registers  $M_3$  to  $M_9$ . The subsequent outputs  $e_2$  to  $e_4$  close the gate circuits  $G_{56}$  to  $G_{62}$  inclusive through the gate circuits  $G_{63}$  to  $G_{64}$  and feed a '0' signal to the inputs of the registers  $M_3$  to  $M_9$ . Consequently, after a total of five shifts, the storage contents of the registers  $M_3$  to  $M_9$  become the bit pattern illustrated in Figure 21.

It will be seen that, regarding the content of the storage section 3C of the register  $M_3$  of Figure 12, i.e. ( $M_3$ , 0) (see Figure 21) its bit is a '1' and therefore this does not become the object of interpolation. The '1' output of the storage section 3C of the register  $M_3$  (Figure 12) closes the gate circuit  $G_{18}$  (Figure 9) and at the same time opens the gate circuit  $G_{19}$ . At this moment the output  $PS_4$  from monostable multivibrator  $N_5$  which has been triggered by the output of the last terminal  $d_5$  of the counter  $C_5$  is fed to the other input of gate circuit  $G_{19}$  through gate circuit  $G_{20}$ . This triggers  $N_1$ , the output  $PS_5$  of which is fed to the gate circuit  $G_{69}$  (Figure 17). The content of the shift register  $R_7$  is shifted by one bit and a '1' is written in the storage section  $X_1$  through the gate circuit  $G_{197}$ . Also the foregoing output  $PS_5$  advances the content of the counter  $C_4$  by '1' through the gate circuit  $G_{54}$  (Figure 11). The counter  $C_4$  is for counting the row magnification of an enlarged dot pattern. The outputs  $h_1$  to  $h_4$  of the counter  $C_4$  which has counted the above-mentioned '1' are fed to the gate circuits  $G_{48}$  to  $G_{51}$ . In this case, since the gate circuits  $G_{48}$  to  $G_{51}$  are opened by the output  $PS_6$  of monostable multivibrator  $N_2$  (Figure 9) which has been triggered by the output  $PS_5$ , the outputs  $h_1$  to  $h_4$  pass through the gate circuits  $G_{48}$  to  $G_{51}$  inclusive and are fed to one input 'q' of the comparison circuit  $P_2$  through the gate circuits  $G_{40}$  to  $G_{43}$  inclusive. The row magnification of '2' stored in the register  $R_1$  (Figure 8) passes through the gate circuits  $G_5$  to  $G_8$  inclusive since the latter circuits are opened by the output  $PS_6$  and is fed to the other inputs 'p' of the comparison circuit  $P_2$  through the gate circuits  $G_{36}$  to  $G_{39}$  inclusive. The set magnification is '2' and the value on the counter  $C_4$  is '1' and thus coincidence is not obtained; therefore, the coincidence output  $p=q$  of the comparison circuit  $P_2$  does not change. However, the foregoing output  $PS_5$  advances the content of the counter  $C_1$  by '1' through the gate circuit  $G_{54}$ . The counter  $C_1$  is for counting the number of bits stored in the register  $R_7$  shown in Figure 17.

The output  $PS_5$  is fed through the gate circuit  $G_{34}$ , multivibrator  $N_2$ , gate circuit  $G_{35}$  and gate circuit  $G_{20}$  to the gate circuit  $G_{19}$  (Figure 9). Since the gate circuit  $G_{19}$  is opened by the '1' output of the storage section 3C of the register  $M_3$ , the output of the gate circuit  $G_{20}$  passes through the gate circuit  $G_{19}$  and triggers  $N_1$ , thus again producing an output  $PS_5$ . This output shifts the register  $R_7$  by one bit through the gate circuit  $G_{69}$  (Figure 17) whereby the '1' output of the storage section 3C is written in the storage sections  $X_1$  and  $X_2$  of the register  $R_7$ . Also the output  $PS_5$  advances by '1' the content of the counter  $C_1$  (Figure 11) so that its count content becomes '2' and, in addition the output  $PS_5$  makes the content of the counter  $C_4$  into '2'. The count outputs  $h_1$  to  $h_4$  are fed to the q input of the comparison circuit  $P_2$  in the same way as hereinbefore described, where they are compared with the row magnification '2'. Since both objects of comparison are '2', a '1' is produced at the output  $p=q$  of the comparison circuit  $P_2$ . As a result an output  $W$  is produced from the gate circuit  $G_{78}$  (Figure 14) and this resets the counter  $C_4$ , through the gate circuit  $G_{56}$  (Figure 11). The output  $W$  also triggers the monostable multivibrator  $N_6$  (Figure 14) thus causing the production of an output  $PS_7$  which goes to  $PS_8$  through the gate circuit  $G_{77}$ , advancing the content of the counter  $C_8$  by '1'.

The output  $PS_8$  is applied as a longitudinal (vertical) shift pulse to the registers  $M_1$  to  $M_9$  shown in Figure 12, causing the contents of the lower rank registers of  $M_1$  to  $M_9$  to be transcribed to the next higher rank registers. The resulting contents are thus made as shown in Figure 22. Consequently, in the storage section 3C of the register  $M_3$  is stored the bit corresponding to the two rows and one column of the matrix in the bit pattern of Figure 20, and this bit becomes the regarded bit. The output  $PS_7$  of multivibrator  $N_6$  (Figure 14) triggers  $N_7$  to produce an output  $PS_9$ , which is fed to the gate circuit  $G_{19}$  through the gate circuit  $G_{20}$  (Figure 9).

Thereafter, in the same manner as hereinbefore described '1' and '1' are stored in the register  $R_7$  of Figure 17. When in this way seven bits, that is, the bits corresponding to the dots of the number of the row and the column of the matrix (z,1) (z being any integer from 1 to 7) shown in Figure 3, have been stored in the register  $R_7$ , an output of '7' is produced from the counter  $C_1$  (Figure 11). Since this output coincides with the '7' stored in the preset counter  $C_2$ , a coincidence output  $PS_{10}$  is produced by the coincidence circuit  $P_1$  and the content of the counter  $C_3$  is advanced by '1'. At the same time, the coincidence output  $PS_{10}$  actuates the wire driving circuit DR shown in Figure 17 so that each wire is driven correspondingly to the stored content of the register  $R_7$ . The wire head continues moving. As the contents of the register  $R_7$  are all '1', all the wires  $PN$  are driven to form the seven dots of the first column shown in Figure 3. After the output  $PS_{10}$  has been fed to the wire driving device DR, an output  $PS_{11}$  is produced from the said device DR. This output  $PS_{11}$  opens the gate circuits  $G_{44}$  to  $G_{47}$  (Figure 11) and the output '1' of the counter  $C_3$  is fed to one q input of the comparison circuit  $P_2$  through the gate circuits  $G_{40}$  to  $G_{43}$  inclusive.

The column magnification '3' stored in the register  $R_2$  is fed to the p inputs of the comparison circuit  $P_2$  through the gate circuits  $G_1$  to  $G_4$  (Figure 8) and  $G_{36}$  to  $G_{39}$  (Figure 11). Since the values compared are different, the output  $p=q$  of the comparison circuit  $P_2$  does not change. Consequently, the gate circuit  $G_{72}$  (Figure 14) produces an output which operates the flip-flop circuit  $F_1$  the output from which opens the gate circuit  $G_{73}$ , so that output from the clock pulse generator CL is fed to the counter  $C_8$  through the gate circuits  $G_{73}$ ,  $G_{76}$  and  $G_{77}$ . As the counter  $C_8$  has already counted shift pulses three times, its content is '3'. If, in addition, six pulses of the foregoing clock pulse are fed in, the value on the counter  $C_8$  becomes '9', and coincidence thereof with the preset value '9' of the counter  $C_9$  is obtained in the coincidence circuit  $P_4$ . This coincidence output  $S_1$  resets the counter  $C_8$  through the gate circuit  $G_{75}$ , and resets the flip-flop circuit  $F_1$  to close the gate circuit  $G_{73}$ , thus causing the supply of clock pulse to the counter  $C_8$  to cease. The aforementioned six pulses through the gate circuit  $G_{77}$  are fed as a longitudinal shift pulse for the registers  $M_1$  to  $M_9$  (Figure 12) and, therefore, the contents of the registers are shifted six times successively from lower rank to higher rank registers. This returns the stored contents of registers  $M_1$  to  $M_9$  to the bit pattern in the initial state shown in Figure 21. In other words the initial stored content has been re-obtained by shifting from the initial stored state nine times. Then the dots in the second column, that is, the dots of the row and column numbers of the matrix (y,2) (y being any integer from 1 to 7), are formed in the same way as above described. At the end of such dot formation, the counter  $C_3$  (Figure 11) counts '2' and this counting output is compared with the magnification '3' by the comparison circuit  $P_2$ . Since the two values do not coincide the output  $p=q$  of the comparison circuit  $P_2$  does not change and the same operation as above described is repeated.

When the dots as far as the third column in Figure 3 have been formed in this way, the value on the counter  $C_3$  (Figure 11) becomes '3'. Coincidence of this value with the column magnification '3' produces a logic '1' in the output  $p=q$  of the comparison circuit  $P_2$  of Figure 11. As a result, an output is produced from the gate circuit  $G_{55}$  a delayed output  $PS_{12}$

delayed by the delay circuit DL resets the counter C<sub>3</sub>. Also, the output PS<sub>12</sub> advances by '1' the content of the counter C<sub>6</sub>. In addition the output PS<sub>12</sub> triggers the multivibrator N<sub>8</sub>, the output of which is fed to the gate circuit G<sub>70</sub>. The output of the coincidence circuit P<sub>3</sub> is now '0' and so the gate circuit G<sub>70</sub> is kept open, which causes an output PS<sub>21</sub> to be produced from multivibrator N<sub>8</sub>. The said output PS<sub>21</sub> advances the value on the counter C<sub>5</sub> by '1' through the gate circuit G<sub>65</sub>, multivibrator N<sub>3</sub> and gate circuit G<sub>66</sub>. Also, when the output PS<sub>2</sub> occurs, the output of the arithmetic unit AD (Figure 10) is transcribed in the memory latch R<sub>5</sub>, the output of which designates a column in the character generator CG (Figure 12). Consequently, the second column shown in Figure 20 is read out from the character generator CG and is stored in the storage sections 3C to 9C of the registers M<sub>3</sub> to M<sub>9</sub>.

Thereafter, dots are formed in the manner above described. If a '0' has been stored in the storage section 3C of the register M<sub>3</sub> shown in Figure 12 this does not result in interpolation in accordance with the methods of the present invention. For example, if the area [5,4] in Figure 3 is blank operation is different from that above described.

Since the content of the storage section 3C is '0' the gate circuit G<sub>18</sub> (Figure 9) is opened and the output of the gate circuit G<sub>20</sub> goes to an output S<sub>0</sub> through the gate circuit G<sub>18</sub>. The output S<sub>0</sub> triggers the monostable multivibrator N<sub>11</sub> (Figure 17) the output of which opens the gate circuit G<sub>136</sub>. Since the example now being considered does not accord with the interpolation methods of this invention, the outputs U<sub>1</sub> to U<sub>4</sub> of the interpolation detecting circuit shown in Figure 16 are '0'. Consequently, the output of the gate circuit G<sub>135</sub> (Figure 17) is '0' and the output of the gate circuit G<sub>136</sub> remains '0', so that the flip-flop circuit F<sub>3</sub> assumes its reset state. As a result, the output of the gate circuit G<sub>137</sub> becomes '0', the output of monostable multivibrator N<sub>12</sub> shifts the register R<sub>7</sub> by one bit and the '0' output of the gate circuit G<sub>137</sub> is written into the register R<sub>7</sub>. Thereafter, the flip-flop circuit F<sub>3</sub> is reset by the output of the monostable multivibrator N<sub>13</sub>.

Assuming that the dots up to the ninth column in the dot pattern shown in Figure 3 have been formed in the same way, the counter shown in Figure 13 now counts '3'.

Accordingly, the column range from the 10th to the 15th columns and the row range from the 1st to the 4th rows in Figure 3 accord with interpolation as above explained in connection with Figures 6 and 7. The interpolation range from the 10th to the 12th columns and from the 3rd to the 4th rows corresponds to Figure 7D. When a blank '0' in such an interpolation range has been stored in the storage section 3C shown in Figure 12, the output U<sub>4</sub> of the interpolation detecting circuit shown in Figure 16 becomes '1' and the outputs U<sub>1</sub> to U<sub>3</sub> become '0'. Whether or not dots should be formed in an interpolation range is decided by the circuit shown in Figure 17. Consider, for example, the matrix area [3,10]. The outputs f<sub>1</sub> to f<sub>4</sub> (hereinafter referred to generically as 'F') of the counter C<sub>3</sub> shown in Figure 11 are '0'; the outputs h<sub>1</sub> to h<sub>4</sub> (hereinafter referred to generically as 'H') of the counter C<sub>4</sub>, also shown in Figure 11 are '0'; the row magnification S is set at '2', and the column magnification T is set at '3', all this data being put in the circuit shown in Figure 17. Consequently, the outputs of the multiplier AC<sub>1</sub> and AC<sub>3</sub> become '0' and the output of the adder B<sub>3</sub> becomes '3'. As a result, the input relationship of the comparator P<sub>8</sub> becomes  $\ell_3 > \ell_4$ , its output becomes '0', and the output of the gate circuit G<sub>133</sub> becomes '0'. Since the other inputs V<sub>1</sub> to V<sub>3</sub> are '0', the output of the gate circuit G<sub>135</sub> becomes '0' and this is stored in the register R<sub>7</sub> in the manner already described.

Now consider, as an example, the matrix area (3,12) shown in Figure 3. For this area the output F of the counter C<sub>3</sub> (Figure 11) is '2'; the output H of the counter C<sub>4</sub> is '0'; and the output of the multiplier AC<sub>1</sub> (Figure 17) is '4', that is  $a_4 = 4$ . Further output of the multiplier AC<sub>3</sub> is '0' and that of the adder B<sub>3</sub> becomes '3', so that the input of the comparator P<sub>8</sub> may be expressed as  $\ell > \ell_3$  and at the output thereof a '1' is produced. The input U<sub>4</sub> of the gate circuit G<sub>133</sub> is a '1' and this is produced at the output of the gate circuit G<sub>133</sub>. Consequently a '1' is produced at the output of the gate circuit G<sub>135</sub>. The gate circuit G<sub>136</sub> is kept open by the output of the monostable multivibrator N<sub>11</sub> (Figure 17) which has been triggered by the output S<sub>0</sub> of the gate circuit G<sub>18</sub> (Figure 11). The resulting output sets the flip-flop circuit F<sub>3</sub> and produces a '1' at one input of the gate circuit G<sub>137</sub>. The pulse from monostable multivibrator N<sub>12</sub> produces a '1' at the output of the gate circuit G<sub>137</sub>; the register R<sub>7</sub> is shifted by one bit through the gate circuit G<sub>69</sub>; and a '1' is written into the register R<sub>7</sub>. This becomes an interpolation dot.

Next, consider the matrix area (4,12) in Figure 3. For this the output F of the counter C<sub>3</sub> is '2' and the output H of the counter C<sub>4</sub> is '1'. Consequently, the output  $\ell_4$  of the multiplier AC<sub>1</sub> is '4', that of the multiplier AC<sub>3</sub> is '3' and, therefore, the output  $\ell_3$  of the adder B<sub>3</sub> becomes '6'. The input relationship of the comparator P<sub>8</sub> becomes  $\ell_4 > \ell_3$  and the output thereof becomes '0', so that the output of the gate circuit G<sub>133</sub> becomes '0' and '0' is written into the register R<sub>7</sub>. Accordingly interpolation is not performed.

Thus whether or not a blank area calls for interpolation by the present invention is detected by the interpolation detecting circuit, and whether or not a dot should be formed in

(15)

the blank area is detected by the upper half circuit of Figure 17 and interpolation is made if necessary.

Figure 18 shows a modification which can be used instead of Figure 17. The devices referenced  $G_{138}$  to  $G_{196}$  are gate circuits;  $N_{14}$  to  $N_{17}$  are monostable multivibrators;  $AC_4$  is a multiplier;  $B_5$  is an adder;  $P_{10}$  is a comparator;  $R_9$  to  $R_{12}$  are registers; and  $TM_1$  and  $TM_2$  are timing pulse generators.

The arrangement of Figure 18 will now be described in the same manner, and with the same examples of operation as were used in explaining Figure 17. As already mentioned, the matrix area (3,12) shown in Figure 3 requires interpolation and the output  $U_4$  of the interpolation detecting circuit is '1'. At the time of detection of this area, the output  $F$  of the counter  $C_3$  shown in Figure 11 is '2' and the output  $H$  of the counter  $C_4$  is '0'. The row magnification  $S$  is '2' and the column magnification  $T$  is '3'. The output  $S_0$  produced from the gate circuit  $G_{118}$  (Figure 9) causes timing pulses to be generated successively at the outputs  $V_1$  to  $V_4$  of the timing pulse generator  $TM_1$  shown in Figure 18. Upon generation of a pulse at the output  $V_1$ , the row magnification  $S=2$  is fed to one input of the multiplier  $AC_4$  through the gate circuits  $G_{138}$  and  $G_{144}$ , and the gate circuit  $G_{143}$  is opened by the said pulse, so that the output  $F=2$  of the counter  $C_3$  is fed to the other input of the multiplier  $AC_4$ . Consequently, a multiplication of '2' by '2' is effected in the multiplier  $AC_4$  to produce '4' at its output, and this '4' is written into the register  $R_9$  by the above-mentioned pulse. Next, upon generation of pulse from the output  $V_2$  of the timing pulse generator  $TM_1$ , the gate circuit  $G_{139}$  is opened and the column magnification  $T=3$  is fed to one input of the multiplier  $AC_4$ . Also the gate circuit  $G_{146}$  is opened and the output  $H=0$  of the counter  $C_4$  is fed to the other input of the multiplier  $AC_4$ . Consequently, a '0' is produced at the output of the multiplier  $AC_4$  and it is written into the register  $R_{10}$  by the pulse of the output at  $V_2$  through the gate circuit  $G_{148}$  which is opened by the said pulse. Further the pulse from the output  $V_3$  of the timing pulse generator  $TM_1$  opens the gate circuits  $G_{140}$  and  $G_{141}$  and the row magnification '2' and the column magnification '3' are fed to the multiplier  $AC_4$  to produce '6' at its output. This is written into the register  $R_{11}$  by the pulse from the output  $V_3$ . Upon generation of a pulse at the output  $V_4$  of the timing pulse generator  $TM_1$ , the gate circuit  $G_{150}$  is opened, but its output is '0' since the output  $U_3$  of the interpolation detecting circuit is '0', and consequently the output of the gate circuit  $G_{157}$  also becomes '0'. As a result, a '0' is written into the register  $R_{12}$  by the output pulse at  $V_4$ . However the gate circuit  $G_{189}$  (Figure 19) is opened by the output pulse at  $V_4$  and a logic invert  $U_3 = '1'$  of the output  $U_3 = 0$  of the interpolation detecting circuit opens the gate circuits  $G_{193}$  and  $G_{194}$  through the gate circuit  $G_{191}$ . With an output  $U_4 = 1$  of the interpolation detecting circuit, a pulse is generated at the output  $V_6$  of the gate circuit  $C_{194}$  and monostable multivibrator  $N_{17}$  is triggered to produce a pulse at the output  $V_7$ . First the gate circuits  $G_{154}$  and  $G_{158}$  are opened by the output pulse at  $V_6$  and the '0' output stored in the register  $R_{10}$  and the column magnification  $T = 3$  are added together by the adder  $B_5$  to produce an output '3', which is written into the register  $R_{12}$  by the pulse at  $V_6$ . Next, the gate circuits  $G_{180}$  and  $G_{184}$  are opened by the pulse at the output  $V_7$  of multivibrator  $N_{17}$  (Figure 19) and '3' is fed into one input 'a' of the comparator  $P_{10}$ , while to the other input 'b' is fed the '4' which has been stored in the register  $R_9$ . Therefore the input relationship in the comparator  $P_{10}$  becomes  $a > b$  and '1' is produced at the output  $a > b$  of the said comparator. Since the output  $a > b$  is '0', the gate circuits  $G_{174}$  through  $G_{176}$  are opened. To the gate circuit  $G_{174}$  is fed the output from  $V_7$  and the gate circuit  $G_{178}$  therefore produces an output which triggers monostable multivibrator  $N_{16}$  through the gate circuit  $G_{196}$  to produce an output pulse  $PS_{15}$ . Subsequent operations are as already explained.

Consider the matrix area (4,12) of Figure 3. For this the output  $U_4$  of the interpolation detecting circuit is '1', the output  $F$  of the counter  $C_3$  is '2' and the output  $H$  of the counter  $C_4$  is '1'. Production of the output  $S_0$  shown in Figure 9 is followed by issuance of timing pulses successively at the outputs  $V_1$ ,  $V_2$ ,  $V_3$  and  $V_4$  of the timing pulse generator  $TM_1$ , and multiplication is done successively by the multiplier  $AC_4$  in the manner already described and '4', '3' and '6' are stored in the registers  $R_9$ ,  $R_{10}$  and  $R_{11}$  respectively. Next, upon generation of a pulse from the output  $V_4$  of the timing pulse generator, a pulse of the output  $V_6$  is produced from the gate circuit  $G_{194}$  through the gate circuits  $G_{189}$  and  $G_{191}$  (Figure 19) and a pulse is produced by the monostable multivibrator  $N_{17}$  at the output  $V_8$ . With production of the pulse at  $V_6$ , the gate circuits  $G_{154}$  and  $G_{158}$  (Figure 18) are opened, and the output '3' of the register  $R_{10}$  and the column magnification  $T = '3'$  are added together by the adder  $B_5$  to produce an output '6', which is stored in the register  $R_{12}$ . Next, with the production of a pulse at the output  $V_7$  produced, the gate circuits  $G_{180}$  and  $G_{184}$  (Figure 19) are opened and '6' and '4' are fed respectively to the inputs 'a' and 'b' of the comparator  $P_{10}$  giving an input relationship of  $a > b$  and causing a '1' to be produced at the output  $a > b$  of said comparator  $P_{10}$ . Consequently, an output  $V_8$  is produced from the gate circuit  $G_{195}$  through the gate circuit  $G_{192}$  which is kept open by the pulse at the output  $V_7$ . The pulse at the

output  $V_8$  causes an output to be produced from the gate circuit  $G_{168}$  and consequently outputs are produced from the gate circuits  $G_{169}$ ,  $G_{171}$  and  $G_{173}$ . The output of the gate circuit  $G_{173}$  triggers monostable multivibrator  $N_{16}$  through the gate circuit  $G_{196}$  to produce an output  $PS_{15}$ . Subsequent operations are as previously explained.

5 Dots and interpolation dots are formed in the manner above described. When the dots of the 15th column shown in Figure 3 have been formed, the counter  $C_6$  shown in Figure 13 counts '5' and coincidence thereof with the '5' count in the preset counter  $C_7$  causes an output to be produced from the coincidence circuit  $P_3$  and fed to the gate circuit  $G_{71}$ . Since the gate circuit  $G_{71}$  is kept open by the output of the monostable multivibrator  $N_8$  which has been triggered by the circuit  $G_{71}$  the counter  $C_6$  is reset and a signal is produced for moving the wire head to the next predetermined position so as to provide spacing for the character to be printed next. This technique is common practice in ordinary wire dot and other head driving type printers and therefore need not be described here.

10 After a part of a character has been formed, a predetermined space is taken and a portion corresponding to  $5 \times 7$  dots of the following letter, numeral or other symbol is formed. When recording by a single line scanning of the head has been completed, the paper is moved on ahead to effect line feed.

15 There will now be given an explanation of the case in which the latter half dots in the dot pattern of Figure 3 are to be formed. Upon completion of dot recording in a single line scanning as above mentioned, a carriage return signal  $ES$  is produced from the wire driving device  $DR$  (Figure 17) by conventional means and the wire head returns to the recording start position. These operations are commonly performed in ordinary wire dot printers and similar recording devices and are per se no part of this invention and are too well known per se to need description here.

20 During the period between the issuance of the foregoing carriage return signal and the return of the wire head to the recording start position, the following preparations are made. When printing by a single head scanning has been completed, that is, after the dots of the last column of the last character have been formed, preparations for the following operation are made by an output  $PS_{17}$  which is produced from the gate circuit  $G_{71}$  shown in Figure 13. When printing corresponding to a single scanning has been completed, the counter  $C$  (Figure 11) counts '1' and the counter  $C_8$  (Figure 14) stores the number of longitudinal shifts of the registers  $M_1$  to  $M_9$ . Therefore, it is necessary to transcribe these contents to latch circuits. First, explanation will be given of the operation for transcribing the content of counter  $C_4$ . The aforementioned output  $PS_{17}$  causes an output to be produced from the gate circuit  $G_{89}$  (Figure 15) to trigger monostable multivibrator  $N_{10}$  and by the resulting output  $PS_{18}$  the '1' in the counter  $C_4$  (Figure 11) is written in the storage latch  $R_6$ .

25 Transcription of the counter  $C_8$  shown in Figure 14 is made in the following manner. The gate circuits  $G_{79}$  to  $G_{82}$  (Figure 15) are opened to allow the storage output from the register  $R_8$  to go to outputs  $K_1$  to  $K_4$  through the gate circuits  $G_{79}$  to  $G_{82}$  inclusive and the outputs  $K_1$  to  $K_4$  are fed to one set of inputs of the arithmetic unit  $AD$  (Figure 10). The content of the storage latch  $R_8$  is kept at '0' while the dots of the initial seven rows of a character are formed and consequently the last mentioned set of inputs of the arithmetic unit  $AD$  receive (0 0 0 0). Further the above-mentioned output  $PS_{18}$  opens the gate circuits  $G_9$  to  $G_{12}$  (Figure 10) to allow the counting output '3' of the counter  $C_8$  (Figure 14) to be fed to the other set of inputs of the arithmetic unit  $AD$ . Consequently, '3' is produced at the output of the arithmetic unit  $AD$  and is written into the storage latch register  $R_8$  (Figure 15) on the cessation of the foregoing output  $PS_{18}$  and thus the content of the counter  $C_8$  shown in Figure 14 is held. The content of the counter  $C_8$  is not directly transcribed to the register  $R_8$  for the following reason. If recording of a character is completed only by two scanings of wire head, as in the present example, there is no problem. If there are more than two scanings, however, it is necessary, on the basis of how many times up to the last time the storage contents of the registers  $M_1$  to  $M_9$  have been shifted in a longitudinal direction, to know at the time of the following scanning from which row of the bit pattern recording must be made in the same character as last time and which has newly been written from the character generator  $CG$ . Consequently the newly written bit pattern must be longitudinally shifted by the corresponding number of times.

30 Upon arrival of the wire head at the start position, the carriage return signal  $ES$  shown in Figure 17 is fed from the wire driving device  $DR$  to the counter  $C_5$  through the gate circuit  $G_{65}$ , multivibrator  $N_3$  and gate circuit  $G_{66}$  (Figure 12) which causes lateral shift pulses of the registers  $M_1$  to  $M_9$  to be produced successively at the output of the counter  $C_5$ , so that the bit pattern corresponding to the dot and blank of each area is again transcribed from the character generator  $CG$  to the registers  $M_1$  to  $M_9$ . The operation up to this point is as already described. The bit pattern stored in the registers  $M_1$  to  $M_9$  corresponds to the dot pattern up to the 7th row in Figure 3. Therefore, in order to form the dots from the 8th to 14th rows, the storage contents of the registers  $M_1$  to  $M_9$  are shifted three times in a

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longitudinal direction. The content of the storage section of register  $M_3$  becomes a '1' bit which corresponds to the dot of the row number and row column of the matrix (4,1) in Figure 2. Then, by the last output of the counter  $C_5$  shown in Figure 12, part of the dot pattern corresponding to the 1st, 2nd and 3rd columns of the dot pattern of Figure 2 is written in the registers  $M_3$  to  $M_9$ . Thereafter, the output  $PS_4$  of multivibrator  $N_5$ , which has been triggered from the terminal  $d_5$  of the counter  $C_5$ , sets the flip-flop circuit  $F_2$  (Figure 14) the output of which opens the gate circuit  $G_{74}$ . Clock pulses from the clock pulse generator CL are fed to the counter  $C_8$  through the gate circuit  $G_{76}$  and the gate circuit  $G_{77}$ , and at the same time the registers  $M_1$  to  $M_9$  are longitudinally shifted. When three pulses have been counted by the counter  $C_8$ , the content '3' of the storage latch  $R_8$  is fed to the coincidence circuit  $P_5$  through the gate circuits  $G_{83}$  to  $G_{86}$  shown (Figure 15). The resulting output  $PS_{19}$  resets the flip-flop circuit  $F_2$  (Figure 14).

In this way the aforementioned three pulses through the gate circuit  $G_{77}$ , shift the contents of the registers  $M_1$  to  $M_9$  three times in a longitudinal direction. Also the content of the storage latch  $R_8$  is set in the counter  $C_4$  by the output  $PS_{19}$ .

In subsequent operations, printing is made in the same manner previously stated and the dots of the 8th and the following rows of Figure 3 are formed. There is thus formed a clear and recognisable letter 'R' as shown in Figure 23 by the addition of the interpolation dots which are shown cross hatched in the said Figure 23.

In the above-mentioned example, the number of wires was seven and the row magnification of a character was '2'. If the magnification is an integral multiple of the number of wires such as 7, 14 and 21, printing is made in the following manner: After the wire head had completed the scanning for magnified bits corresponding to one bit in the original pattern and when it has shifted to the following scanning, printing is made from the first of the magnified bits of the bits of the following row in the original pattern. An explanation on this operation is given below.

If the row magnification is to be '14', the counters  $C_4$  and  $C_3$  shown in Figure 11 must be changed to tetradecimal counters. Assuming that by two scanings of the wire head, recording corresponding to 14 dots has been made and thus magnification of one dot in the original pattern has been completed, the counter  $C_4$  now counts '0' and the counter  $C_3$  also counts '0'. Since the decoder DC shown in Figure 15 is so designed as to produce an output when magnification is 1, 7, 14, 21 ..., the gate circuit  $G_{90}$  shown in Figure 15 is kept open. Therefore, when the output of the comparison circuit  $P_2$  shown in Figure 11 becomes  $P = Q$ , an output is produced from the gate circuit  $G_{90}$  and causes the gate circuit  $G_{88}$  to be opened. However a signal (DC) which indicates the last character for a single scanning is advance programmed as part of the data so that, after the output of the last character has been produced, the said indication signal DC triggers multivibrator  $N_9$  through the gate circuit  $G_{88}$  to produce an output  $PS_{20}$  which resets the counter  $C_4$  through the gate circuit  $G_{52}$  (Figure 11) and also adds '1' to the counter  $C_8$  shown in Figure 14. Subsequent operations are as previously explained.

Although in the embodiments described and illustrated monostable multivibrators have been shown they are clearly not essential to the invention and timing pulses may be produced in other ways known per se e.g. from reference clock pulse sources.

The invention is not limited to its application to wire dot printers, but is applicable to other forms of printer e.g. to electronic printers such as electro-sensitive printers which record letters, numerals and other characters or symbols in the form of dot matrices.

In the particular embodiments described and illustrated the number of dot-forming elements (wires) was seven but obviously the invention is not limited to this number and there may be any suitable number of dot-forming elements provided, of course, that appropriate changes are made in the design of the apparatus to accommodate the changed number of elements.

Again, in the particular embodiments described and illustrated the row and column magnifications were set to 2 and 3 respectively; therefore, as shown in Figure 23, the number of interpolation dots in each area of interpolation was one. However, increase in magnification should be, for best results, accompanied by an increase in the number of interpolation dots. This is exemplified by Figure 20, in which interpolation dots have been shown with a bit pattern of '1' and '0' under the condition of row magnification  $S = 2$  and column magnification  $T = 3$ , the mode shown in Figure 7B being taken. In Figure 20, '1' indicates an interpolation dot and '0' indicates a blank portion.

For determining the number of dots in the example described with reference to the drawings, dots were experimentally formed and empirical formulae were obtained for those found to give high character clarity. However, with respect to the number and position of dots formed, not only in the present example but also in other examples, various cases may be considered according to the way in which the character concerned is recognised. In the present example, an interpolation dot was included in one range out of two ranges defined

by a diagonal line. For example, however, even if an interpolation dot is formed so that it is included also in the other range beyond the diagonal line, the clearness of the character concerned will not greatly lower. In order to form dots in such a manner, corresponding empirical formulae may be prepared and an operational circuit made in accordance with these formulae. The outputs of an operational circuit thus made may be used (instead of the outputs of the operational circuit which are fed to the gate circuits  $G_{131}$  to  $G_{134}$  shown in Figure 17) and fed to the said gate circuits  $G_{131}$  to  $G_{134}$ .

In another modification the number and position of interpolation dots to be formed as well as the magnification of a character are programmed in a memory and, with the aid of the memorised data and of the outputs  $U_1$  to  $U_4$  of the interpolation detecting circuit  $U$ , dots may be formed in the interpolation ranges programmed for interpolation. In this case, as in others, the number and position of dots to be formed in the ranges requiring interpolation may be suitably set as necessary.

As will now be seen the present invention results in the formation of dot characters such as letters, numerals or other symbols which have been enlarged with required magnifications in both row and column directions, but which nevertheless, despite possibly quite large magnifications, retain good clarity and recognisability by reason of the insertion of interpolation dots.

#### WHAT WE CLAIM IS:-

1. An apparatus for magnifying an original letter, numeral or other symbol or character in dot matrix form comprising: storage means for storing a bit pattern in which dots forming said character or symbol and non-dots (blanks) are converted into bits of a first logic value and into bits of a second logic value respectively; matrix row magnification setting means and matrix column magnification setting means for setting desired row and column magnifications respectively of the character or symbol to be recorded; first means for reading out the bits which constitute data stored in said storage means; selecting means for selecting the respective bits in accordance with a predetermined order; first magnification converting means for forming bits each of which has the same logic value as the selected bit and the number of which is equal to that set in said matrix row magnification setting means; second magnification converting means for forming bits each of which has the same logic value as the selected bit and the number of which is equal to that set in said matrix column magnification setting means; and second means for recording a magnified dot symbol or character in accordance with the respective bits formed by said first and second magnification converting means.

2. An apparatus for magnifying and clarifying an original letter, numeral or other symbol or character in dot matrix form comprising: storage means for storing a bit pattern in which dots forming said character or symbol and non-dots (blanks) are converted into bits of a first logic value and of a second logic value respectively; matrix row magnification setting means and matrix column magnification setting means for setting desired row and column magnifications respectively of the character or symbol to be recorded; first means for reading out the bits which constitute data stored in said storage means; selecting means for selecting the respective bits in accordance with a predetermined order; detecting means for detecting whether or not the array of a bit having the second logic value selected by said selecting means and surrounding bits thereof coincides with a predetermined rule and, if such coincidence is detected, converting the selected bit into a bit having the first logic value; first magnification converting means for forming bits each of which has the first logic value when the selected bit coincides with the first logic value or with the second logic value to be converted by said detecting means and has the second logic value when the selected bit is not converted by said detecting means and the number of which coincides with that set in said matrix row magnification setting means; second magnification converting means for forming bits each of which has the first logic value when the selected bit coincides with the first logic value or with the second logic value to be converted by said detecting means and has the second logic value when the selected bit is not converted by said detecting means and the number of which coincides with that set in said matrix column magnification setting means; and second means for recording a magnified dot symbol or character in accordance with the respective bits formed by said first and second magnification converting means.

3. An apparatus as claimed in claim 2, wherein said detecting means comprises: means for detecting whether there is satisfaction of the condition that in the aforesaid bit pattern two bits of said first logic value adjoin in an oblique direction and that each of two bits of said second logic value adjoins each of the aforementioned two bits of the first logic value; and means for converting one of said two bits of the second logic value if satisfaction of said condition is detected.

4. An apparatus as claimed in claim 2 or 3 wherein said detecting means comprises: means for detecting whether there is satisfaction of the condition that in an arbitrary three bits of said first logic value, the first, second and third bits are formed in an oblique direction,

by a diagonal line. For example, however, even if an interpolation dot is formed so that it is included also in the other range beyond the diagonal line, the clearness of the character concerned will not greatly lower. In order to form dots in such a manner, corresponding empirical formulae may be prepared and an operational circuit made in accordance with these formulae. The outputs of an operational circuit thus made may be used (instead of the outputs of the operational circuit which are fed to the gate circuits  $G_{131}$  to  $G_{134}$  shown in Figure 17) and fed to the said gate circuits  $G_{131}$  to  $G_{134}$ .

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As will now be seen the present invention results in the formation of dot characters such as letters, numerals or other symbols which have been enlarged with required magnifications in both row and column directions, but which nevertheless, despite possibly quite large magnifications, retain good clarity and recognisability by reason of the insertion of interpolation dots.

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2. An apparatus for magnifying and clarifying an original letter, numeral or other symbol or character in dot matrix form comprising: storage means for storing a bit pattern in which dots forming said character or symbol and non-dots (blanks) are converted into bits of a first logic value and of a second logic value respectively; matrix row magnification setting means and matrix column magnification setting means for setting desired row and column magnifications respectively of the character or symbol to be recorded; first means for reading out the bits which constitute data stored in said storage means; selecting means for selecting the respective bits in accordance with a predetermined order; detecting means for detecting whether or not the array of a bit having the second logic value selected by said selecting means and surrounding bits thereof coincides with a predetermined rule and, if such coincidence is detected, converting the selected bit into a bit having the first logic value; first magnification converting means for forming bits each of which has the first logic value when the selected bit coincides with the first logic value or with the second logic value to be converted by said detecting means and has the second logic value when the selected bit is not converted by said detecting means and the number of which coincides with that set in said matrix row magnification setting means; second magnification converting means for forming bits each of which has the first logic value when the selected bit coincides with the first logic value or with the second logic value to be converted by said detecting means and has the second logic value when the selected bit is not converted by said detecting means and the number of which coincides with that set in said matrix column magnification setting means; and second means for recording a magnified dot symbol or character in accordance with the respective bits formed by said first and second magnification converting means.

3. An apparatus as claimed in claim 2, wherein said detecting means comprises: means for detecting whether there is satisfaction of the condition that in the aforesaid bit pattern two bits of said first logic value adjoin in an oblique direction and that each of two bits of said second logic value adjoins each of the aforementioned two bits of the first logic value; and means for converting one of said two bits of the second logic value if satisfaction of said condition is detected.

4. An apparatus as claimed in claim 2 or 3 wherein said detecting means comprises: means for detecting whether there is satisfaction of the condition that in an arbitrary three bits of said first logic value, the first, second and third bits are formed in an oblique direction,



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and that two other bits of said first logic value are formed in a row or in a column direction such that one bit of said two other bits adjoins said one bit, and that the angle between the aforementioned oblique and row or column directions is within 90°; and means for converting one bit of the second logic value which adjoins said first and second bits into a bit of the first logic value if satisfaction of said condition is detected.

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5. Apparatus for arbitrarily magnifying and recording original letters, numerals or other symbols or characters in dot matrix form substantially as herein described with reference to the accompanying drawings.

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