

"Static type semiconductor random access memory".

The present invention relates to a static type semiconductor random access memory (hereinafter referred to as a "static RAM").

In a static RAM, a pair of information complementary to each other as derived from a memory cell are respectively transmitted to a sense amplifier through a pair of data lines and a pair of common data lines CDL and $\overline{\text{CDL}}$. The sense amplifier amplifies the potential difference between the pair of common data lines having developed in accordance with the pair of information, and transmits the output signal of high level or low level to a data output buffer. The data output buffer detects on the basis of its logic threshold voltage whether the output signal from the sense amplifier is at the high level or at the low level, and it delivers the output data of the high level or the low level out of the static RAM in accordance with the detected result.

In "NIKKEI ELECTRONICS 1980 3. 7.",
page 142, Figure 12, by YASUI et al., there is
disclosed as the above mentioned sense amplifier,
a differential amplifier circuit which is constituted
5 by a pair of insulated gate field effect transistors
(hereinafter referred to as "MISFETS") coupled in
the differential mode, and a current mirror circuit
(active load) forming the load of the MISFETS.
In this sense amplifier, the output signal is
10 formed on the basis of current equal to the
difference between the drain currents of the pair
of MISFETS coupled in the differential mode.
Therefore, the sensitivity of this sense amplifier
can be made comparatively high. Moreover, since
15 the load constituting the differential amplifier
circuit is the active load, the gain of the
differential amplifier circuit itself can also be
made comparatively great, for example, about 5.
In order to render the operation of the static RAM
20 faster, however, a sense amplifier having a still
higher gain is requested for reasons stated below.

Since the pair of data lines have a
large number of memory cells coupled thereto, they
have comparatively large parasitic capacitances in
25 themselves. In a static RAM of enlarged memory

capacity, the pair of common data lines become relatively long, so that the pair of common data lines also have comparatively large storage capacitances. Therefore, when the information of the memory cell are read out, potential changes to be applied to the pair of data lines by the memory cell have their changing rates limited by the parasitic capacitances. Similarly, potential changes to be applied from the pair of data lines to the pair of common data lines are limited by the storage capacitances of the latter. In other words, the potential difference which is applied between the pair of common data lines in accordance with the information read out from the memory cell only becomes high comparatively slowly.

Although the sense amplifier referred to above has a comparatively high gain, this gain is still unsatisfactory for the sense amplifier of the large-capacity static RAM. Therefore, when the potential difference between the pair of common data lines has reached a comparatively high value, an output signal capable of driving the data output buffer is first provided from the sense amplifier. A comparatively long time is accordingly required before the data output buffer comes into operation after the information complementary to each other have been delivered

from the memory cell to the pair of data lines.

Moreover, in the above referred to sense amplifier, the differential amplifier circuit is a dissymmetric type differential amplifier circuit which receives a pair of input signals complementary to each other and which forms a single output signal having a potential relative to earth of the circuit as corresponds to the potential difference between the input signals. In consequence, the data output buffer detects the potential of the output signal from the sense amplifier on the basis of its logic threshold voltage relative to earth. In this respect, however, the characteristics of elements constituting the data output buffer will vary due to variations in manufacturing conditions and techniques. The variation of the characteristics of the elements results in the variation of the logic threshold voltages of data output buffers. In order to prevent any malfunction of the static RAM attributed to such variation of the logic threshold voltage of the data output buffer, the sense amplifier should desirably form an output signal of the largest possible amplitude. Since, however, the gain of the sense amplifier is not very high, the potential difference between the pair of common data lines must

be still greater in order to form an output signal of the large amplitude. Therefore, yet a longer time is taken before the data output buffer is operated. The operating speed of the static RAM has accordingly been limited.

In addition, the characteristics of elements constituting the sense amplifier vary due to variations in manufacturing conditions and techniques. It turns out that the sense amplifier has an offset. The sense amplifier is accordingly disadvantageous in that an offset voltage caused by the offset is transmitted to the data output buffer as it is.

For the above reasons, in the case where the above mentioned sense amplifier is employed, the output buffer cannot be driven by the sense amplifier until the potential difference between the pair of common data lines CDL and $\overline{\text{CDL}}$ reaches such a comparatively great value as 0.5 volt. This is a serious disadvantage to achieving the high-speed operation of the static RAM.

According to the present invention there is provided a static type semiconductor random access memory including: memory cells each of which delivers a pair of signals complementary to each other; a first dissymmetric type differential amplifier circuit whose non-inverting input terminal is supplied with one signal of the pair of complementary signals,

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whose inverting input terminal is supplied with the other signal of the pair of complementary signals and which forms a first output signal in-phase with the signal supplied to the non-inverting input terminal;

5 a second dissymmetric type differential amplifier circuit whose inverting input terminal is supplied with said one signal, whose non-inverting input terminal is supplied with the other signal and which forms a second output signal in-phase with said signal supplied

10 to said non-inverting input terminal; and first means supplied with the first output signal and the second output signal for forming a third output signal based on the first output signal and said second output signal.

15 The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:-

Figure 1 is a block diagram of a static memory system;

20 Figure 2A is a block diagram of the internal arrangement of a preferred form of a static RAM, whilst

Figures 2B and 2C are waveform diagrams of the static RAM shown in Figure 2A;

25 Figure 3A is a block diagram of the internal arrangement of a second form of a static RAM whilst

Figures 3B and 3C are waveform diagrams of the static RAM shown in Figure 3A;

Figure 4 is a circuit diagram of a memory cell of 1 bit in a memory cell array;

5 Figure 5 is a circuit diagram of a data output buffer;

Figure 6 is a circuit diagram of a first form of a sense amplifier;

10 Figure 7 is a block diagram of a second form of sense amplifier;

Figure 8 is a circuit diagram of a dissymmetric type differential amplifier circuit constituting a third form of sense amplifier; and

15 Figure 9 is a layout diagram of the principal portions of the sense amplifier.

The arrangement of a static memory system will be described with reference to Figure 1. The static memory system is generally enclosed with a broken line. This system includes an S-RAM IC ARRAY (hereinafter referred to as a "S-RAM") constituted by a plurality of static RAMs, a central processing unit (hereinafter referred to as a "CPU", and not shown) in a computer, and interface circuits between the S-RAM and the CPU. A power circuit E is provided which has a back-up function. A power supply E_0 is formed by a device which steps down and rectifies the mains A.C. voltage, whilst a power supply E_B is constituted by

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a battery. Usually, the supply voltage of the system is fed from the power supply E_0 . When the power supply E_0 has been turned "off" or when it is inoperative due to a fault, the supply voltage of the system is fed from the auxiliary power supply E_B . Thus, even when the main power supply E_0 has been turned "off", the stored contents of the memory chip are retained by the auxiliary power supply E_B . Supply voltages V_{CC} and V_{SS} are common to all the static RAMs.

Next, the input/output signals between the static memory system and the CPU will be explained in greater detail. Address signals A_0 to A_k are signals for selecting a plurality of desired memory cells from among 2^k memory cells in the S-RAM enclosed with a solid line. Among them, the address signals A_0 to A_1 are allotted as address signals common to the various static RAMs, while the address signals A_{i+1} to A_k are allotted as signals for selecting m rows of IC arrays and are used as chip select signals $\overline{CS}$ common to the static RAMs of the respective row. $\overline{WE}$ indicates a write enable signal, which is a signal for the reading and writing instructions of data in the S-RAM and which is fed to the $\overline{WE}$ terminals of all the static RAMs. MS indicates a memory start signal which starts the memory operation

of the S-RAM. D_1 to D_8 indicate input/output data on data bus lines which connect the CPU and the S-RAM.

Now, the static memory system will be described on the S-RAM and the interface circuits separately.

5 First, the S-RAM is constructed of the IC array in which the static RAMs each having a memory capacity of $n \cdot k$ bits (Hereinbelow, the RAM shall be termed "n.k-static RAM". 1 kbits denote $2^{10} = 1024$ bits.) are arrayed to the number of m in each column and
10 to the number of B in each row and are connected in the shape of a matrix of $(n \times m)$ words $\times$ B bits. The data input terminals D_{in} and data output terminals D_{out} of the static RAMs in each of the B columns are respectively connected in common.

15 Secondly, the interface circuits will be described. ADR denotes an address receiver which receives the address signals A_0 to A_k transmitted from the CPU and which converts them into the address signals of timings adapted for the operations of the S-RAM.

20 DCR denotes a decoder which transmits chip select control signals (hereinbelow, termed " $\overline{CS}_1$ to $\overline{CS}_m$ " where $m = 2^k - 1$) for selecting the static RAMs instructed by the address signals A_{i+1} to A_k from among the plurality of static RAMs constituting the S-RAM.

25 DBD indicates a data bus driver whose data input/output

between the CPU and the S-RAM are changed-over by a gate control signal GC. The gate control signal GC is formed by the logical combination between the write enable signal $\overline{WE}$ and the memory start signal MS.

5 Data output signals D_{O1} to D_{OB} from the IC array are output signals which are read out from the data output terminals of the static RAMs (numbering B) of selected row and which are supplied to the DBD. Data input signals D_{I1} to D_{IB} to the IC array
10 are data to be written into desired memory cells, and they are delivered from the DBD and supplied to the data input terminals D_{in} of the static RAMs (numbering B) of the selected row.

15 Now, the functions of the address signals within the static memory system will be explained.

20 The address signals A_0 to A_k from the CPU are classified into two sorts. The address signals A_0 to A_1 are used as address signals for selecting a desired memory cell from within a memory matrix constructed of a plurality of memory cells, in each of the static RAMs constituting the S-RAM. On the other hand, the
25 address signals A_{1+1} to A_k are used as the chip select signal concerning whether or not the whole static RAM is selected as viewed from each of the static RAMs constituting the S-RAM.

Figure 2A shows the internal arrangement of a static RAM which has a memory capacity of 16 kbits and whose input and output operations are executed in single bit unit.

This static RAM of 16 kbits includes four matrices (memory arrays M-ARY1 to M-ARY4) all having equal memory capacities. In each matrix, memory cells are arrayed into 128 rows x 32 columns. Therefore, each of the matrices has the memory capacity of 4096 bits (4 kbits). The matrices are dividedly arranged in such a manner that two of them lie on each of the right and left sides of a row decoder R-DCR.

$2^8 = 256$ decoded output signals which are obtained on the basis of the address signals A_0 to A_5 , A_{12} and A_{13} are respectively transmitted from the row decoder R-DCR to the address selecting lines of rows (word lines WL1 to WL128 and WR1 to WR128).

In this manner, each of the memory cells M-CEL constituting the respective matrices is connected to any one of the word lines WL1 to WL128 and WR1 to WR128 and any one pair of pairs of complementary data lines D_{11} , $\bar{D}_{11}$ to D_{132} , $\bar{D}_{132}$ to be described later.

The address signals A_5 and A_6 are used for selecting

only one of the four memory matrices. In order to select one column in the selected memory matrix, the address signals A_7 to A_{11} are used.

5 A circuit GS receives the address signals A_5 and A_6 , and forms four sorts of memory matrix selecting signals m_1 to m_4 corresponding to these address signals.

Each of column decoders C-DCR1 to C-DCR4 delivers $2^5 = 32$ decoded output signals for selecting columns, on the basis of the address signals A_7 to A_{11} .

10 In a reading operation, a pair of common data lines CDL and $\overline{CDL}$ are divided into four in correspondence with the respective memory arrays by transistors to divide the common data lines ($Q_1, \overline{Q_1}; \dots; Q_4, \overline{Q_4}$), while in a writing operation, the pair of common data
15 lines CDL and $\overline{CDL}$ are coupled in common.

Sense amplifiers SA1, SA2, SA3 and SA4 are respectively arranged in correspondence with the divided parts of the pair of common data lines CDL and $\overline{CDL}$.

To divide the pair of common data lines CDL and $\overline{CDL}$ and equip the respective divided parts with the
20 sense amplifiers SA1, SA2, SA3 and SA4 in this manner, is intended to divide the storage capacitances of the pair of common data lines CDL and $\overline{CDL}$ so as to render the reading operation fast.

25 An address buffer ADB prepares 14 pairs of complemental

address signals a_0 to a_{13} from the 14 external address signals A_0 to A_{13} , respectively, and delivers them to the decoder circuits (R-DCR, C-DCR and GS).

5 An internal control signal generating circuit COM-GE receives the two external control signals $\overline{CS}$ (chip select signal) and $\overline{WE}$ (write enable signal), and delivers signals CS_1 (row decoder control signal), SAC (sense amplifier control signal), we (writing control signal), DOC (data output buffer control signal)
10 and DIC (data input buffer control signal).

The circuit operation of the static RAM shown in Figure 2A will be described with reference to the waveform diagrams shown in Figures 2B and 2C.

15 All operations in the static RAM, that is, an address setting operation, the reading operation and the writing operation are carried out only in the interval in which one external control signal $\overline{CS}$ is at the low level. Herein, the reading operation is executed when the other external control signal $\overline{WE}$
20 is at the high level, and the writing operation is executed when it is at the low level.

First, the address setting operation and the reading operation will be described.

In the case where the external control signal $\overline{CS}$ is at the low level, the address setting operation is continually executed on the basis of the address signals applied during this interval. By keeping the external control signal $\overline{CS}$ at the high level contrariwise, the address setting operation and the reading operation based on indefinite address signals can be prevented.

When the external control signal $\overline{CS}$ has become the low level, the internal control signal generator COM-GE generates the internal control signal CS1 of the high level in synchronism with this signal $\overline{CS}$. The row decoder R-DCR starts its operation by receiving this internal control signal CS1 of the high level. The row decoder (serving also as a word driver) R-DCR decodes the 8 sorts of pairs of complemental address signals a_0 to a_5 , a_{12} and a_{13} supplied from the address buffer ADB, and it selects one word line from among the plurality of word lines and drives it to the high level.

On the other hand, any one of the 4 memory arrays M-ARY1 to M-ARY4 is selected by the memory array selecting signals m_1 to m_4 . In the selected memory array (for example, M-ARY1), one pair of complemental data lines (for example, D11 and $\overline{D11}$) are selected by the column decoder (for example, C-DCR1). More specifically,

when the memory array M-ARY1 has been selected by the memory selecting signal m_1 , the column decoder C-DCR1 starts its operation in response to the selecting signal m_1 . The column decoder C-DCR1 decodes the
5 5 sorts of pairs of complementary address signals a_7 to a_{11} supplied from the address buffer ADB, and brings one decoded output signal for column selection into the high level. In the above example, MISFETs Q_{11} and $\overline{Q_{11}}$
10 are brought into the "on" states by the decoded output signal for column selection. Thus, one pair of complementary data lines (D_{11} and $\overline{D_{11}}$) are selected.

In this way, one memory cell coupled to one word line and one pair of complementary data lines selected is selected (address setting).

15 An information having been stored in the memory cell selected by the address setting operation is delivered to one pair of divided parts of the pair of common data lines, and is amplified by the sense amplifier (for example, SA1).

20 In this case, any one of the 4 sense amplifiers SA1, SA2, SA3 and SA4 is selected by the memory array selecting signals m_1 to m_4 . Only the selected sense amplifier operates during the interval during which the internal control signal SAC of the high level
25 is received.

In this manner, the three sense amplifiers which need not be used among the four sense amplifiers SA1, SA2, SA3 and SA4 are held in the non-operating states, whereby the power dissipation of the static RAM can be rendered low. The outputs of the three sense amplifiers in the non-operating states are held in high impedance (floating) states.

The output signal of the sense amplifier is amplified by the data output buffer DOB, and is transmitted to outside the static RAM as output data D_{out} .

The data output buffer DOB operates only during the interval during which the control signal DOC of the high level is received.

Next, the writing operation will be described.

When the external control signal $\overline{WE}$ has become the low level, the control signal $\overline{we}$ of the high level synchronous therewith is supplied from the internal control signal generator COM-GE to the transistors to divide the common data lines ($Q_1, \overline{Q}_1; \dots; Q_4, \overline{Q}_4$). Since all the transistors for dividing the common data lines are thus brought into the "on" states, the pair of common data lines having been divided in the reading operation are coupled in the writing operation. That is, in the writing operation, the common data line CDL becomes a single common data line coupled

electrically, and the common data line $\overline{CDL}$ similarly becomes a single common data line coupled electrically.

On the other hand, a data input buffer DIB amplifies an input data signal D_{in} from outside the static RAM and delivers the amplified signal to the pair of common data lines CDL and $\overline{CDL}$ coupled in common, during the interval during which the control signal DIC of the low level is received.

The input data signals transmitted to the pair of common data lines CDL and $\overline{CDL}$ are written into the single memory cell M-CEL set by the address setting operation.

Figure 3A shows the internal arrangement of a static RAM which has a memory capacity of 16 kbits and whose input and output operations are executed in 8 bit unit.

This memory IC of 16 kbits includes eight matrices (memory arrays M-ARY1 to M-ARY8) all having equal memory capacities. In each matrix, memory cells are arrayed into 128 rows x 16 columns. Therefore, each of the matrices has the memory capacity of 2048 bits (2k bits). As shown in the figure, the matrices are dividedly arranged in such a manner that four of them lie on each of

the right and left sides of a row decoder R-DCR.

5 $2^7 = 128$ decoded output signals which are obtained on the basis of the address signals A_0 to A_6 are respectively transmitted from the row decoder R-DCR to the address selecting lines of rows (word lines WL1 to WL128 and WR1 to WR128).

10 In this manner, each of the memory cells M-CEL of the respective matrices is connected to any one of the word lines WL1 to WL128 and WR1 to WR128 and any one pair of pairs of complemental data lines D11, $\bar{D}11$ to D132, $\bar{D}132$ to be described later.

15 Word-line intermediate buffers MB1 and MB2 have amplification actions in order to reduce to the utmost delay times at the ends of the word lines WL1 to WL128 and WR1 to WR128, and are interposed between the memory arrays M-ARY2 and M-ARY3 and those M-ARY6 and M-ARY7, respectively.

20 The address signals A_7 to A_{10} are used for selecting one pair of complemental data lines from each of the eight matrices.

 A column decoder C-DCR delivers $2^4 = 16$ decoded output signals for selecting columns, on the basis of the address signals A_7 to A_{10} .

25 An address buffer ADB prepares 11 pairs of complemental address signals a_0 to a_{10} from the 11 external address

signals A_0 to A_{10} , respectively, and delivers them to the decoder circuits (R-DCR and C-DCR).

5 An internal control signal generating circuit COM-GE receives three external control signals $\overline{CS}$ (chip select signal), $\overline{WE}$ (write enable signal) and $\overline{OE}$ (output enable signal), and delivers signals CS1 (row decoder control signal), CS12 (sense amplifier and data input buffer-control signal), W.C. (writing control signal) and $\overline{W.C.O.}$ (data output buffer-control signal).

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The circuit operation of the static RAM shown in Figure 3A will be described with reference to the waveform diagrams shown in Figures 3B and 3C.

15 All operations in the static RAM, that is, the address setting operation, the reading operation and the writing operation are carried out only in the interval in which the external control signal $\overline{CS}$ is at the low level. Herein, the reading operation is conducted when the other external control signal $\overline{WE}$ is at the high level, and the writing operation

20 when it is at the low level.

The external control signal $\overline{OE}$ is used for controlling an output timing in the case of transmitting an output

signal of 8 bits out of the static RAM.

First, the address setting operation and the reading operation will be described.

5 In the case where the external control signal $\overline{CS}$ is at the low level, the address setting operation is continually executed on the basis of the signals applied during this interval. By keeping the external control signal $\overline{CS}$ at the high level contrariwise, the address setting operation and the reading operation based on indefinite
10 address signals can be prevented.

 When the external control signal $\overline{CS}$ has become the low level, the internal control signal CS_1 of the high level synchronous with this signal $\overline{CS}$ is provided from the internal control signal generator
15 COM-GE. Upon receiving the internal control signal CS_1 of the high level, the row decoder R-DCR starts its operation. The row decoder (serving also as a word driver) R-DCR decodes the 7 sorts of pairs of complementary address signals a_0 to a_6 supplied from
20 the address buffer ADB, and it selects one pair of right and left word lines from among the plurality of word lines and drives them to the high level.

 On the other hand, the column decoder C-DCR selects one column from each of the 8 memory arrays M-ARY1
25 to M-ARY8. That is, the column decoder C-DCR decodes

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the pairs of complementary address signals a_7 to a_{10} supplied from the address buffer ADB, and it provides decoded output signals for column selection as select one column from each of the respective memory arrays. One pair of complementary data lines are selected from each memory array by these decoded output signals for column selection.

In this way, eight memory cells coupled to the selected word lines and the pairs of complementary data lines selected for the respective memory arrays are selected (address setting). That is, one memory cell is selected in each memory array.

Information of the memory cells selected by the address setting operation are delivered to the pairs of common data lines CDL and $\overline{CDL}$ of the respective memory arrays, and are amplified by the respective sense amplifiers SA.

The sense amplifiers SA begin to operate in response to the fact that the control signal CS12 becomes the high level in synchronism with the external control signal $\overline{CS}$. It continues to operate during the interval during which this signal CS12 is at the high level.

The output signals of the sense amplifiers SA are amplified by data output buffers DOB, and are transmitted out of the static RAM as output data D_{out1}

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to D_{out8} .

By the way, the data output buffers DOB operate during the interval during which the control signal $\overline{w.c.o}$ of the high level is received.

5 Next, the writing operation will be described.

When both the external control signals $\overline{WE}$ and $\overline{CS}$ have become the low level, the internal control signal generator COM-GE synchronously supplies the control signal $w.c.$ of the high level to writing control transistors ($Q_1, \overline{Q_1}; \dots; Q_4, \overline{Q_4}$). Thus, the writing control transistors are brought into the "on" states, and the respective pairs of common data lines CDL and $\overline{CDL}$ and the corresponding data input buffers DIB are coupled.

15 On the other hand, the data input buffers DIB arranged in correspondence with the respective memory arrays amplify the 8 input data signals D_{in1} to D_{in8} applied from outside the static RAM, respectively, and transmit the amplified signals to the pairs of common data lines CDL and $\overline{CDL}$ arranged in correspondence with the respective memory arrays, during the interval during which the control signal CS12 of the low level is received.

20 The input data signals transmitted to the pairs of common data lines are respectively written into

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the 8 memory cells M-CEL set by the address setting operation.

Figure 4 shows the circuit of the memory cell M-CEL of 1 bit in the memory array of Figure 2A or Figure 3A. This memory cell is constructed of a flip-flop in which the inputs and outputs of a pair of inverter circuits consisting of load resistors R_1 , R_2 and driving MISFETs Q_1 , Q_2 connected in series are cross-connected, and a pair of MISFETs Q_3 , Q_4 for transmission gates. The flip-flop is used as means for storing information, the transmission gate MISFETs are used as addressing means for controlling the transmission of information between the flip-flop and the pair of complementary data lines D and $\bar{D}$ (D_{11} , $\bar{D}_{11}$;; D_{132} , $\bar{D}_{132}$), and the operations thereof are controlled by the address signal applied to the word line W ($WL1$, $WL128$, $WR1$, $WR128$) connected to the row decoder R-DCR.

Figure 5 shows a peripheral circuit, for example, the data output buffer DOB in Figure 2A or Figure 3A. With the data output buffer DOB, when a control signal Cont is logic "1" ($+V_{cc}$), an output V_{out} becomes a logic value conforming with an input signal In, and a very low output impedance is obtained. In contrast,

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when the control signal Cont is "0", the output V_{out} of the data output buffer DCB becomes an indefinite level independent of the input signal In, that is, a very high output impedance is obtained. The buffer having both the high and low output impedances in this manner, makes it possible to form wired-OR among the output signals of a plurality of buffers.

In the final stage, a bipolar transistor Q_{105} of great drivability is used so that a heavy load can be driven at high speed. This bipolar transistor Q_{105} constructs a push-pull circuit along with an N-channel MISFET Q_{106} which is greater in drivability than a P-channel MISFET. As the above control signal Cont, there is used the signal D_{oc} or $\bar{W}.C.O.$ stated before.

Figure 6 is a circuit diagram showing an embodiment of the sense amplifier SA for use in the foregoing static RAM.

In this embodiment, the sense amplifier SA is constructed of a first dissymmetric type differential amplifier circuit P_1 which is composed of a pair of MISFETs Q_{201} and Q_{202} coupled in the differential mode, and active load MISFETs Q_{203} and Q_{204} connected to the drains of the respective differential MISFETs and constituting a current mirror circuit; a second

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dissymmetric type differential amplifier circuit P_2 which is composed of MISFETs Q_{205} to Q_{208} which has the same arrangement as that of the dissymmetric type differential amplifier circuit P_1 ; and a third dissymmetric type differential amplifier circuit P_3 which is composed of MISFETs Q_{210} to Q_{214} and which has the same arrangement as that of the dissymmetric type differential amplifier circuit P_1 or P_2 .

The first and second dissymmetric type differential amplifier circuits P_1 and P_2 receive ^{the} signals D_i and $\overline{D_i}$ from the pair of common data lines CDL and $\overline{CDL}$, respectively. The first dissymmetric type differential amplifier circuit P_1 an output signal $\overline{D_i'}$ whose potential changes in the same direction (in-phase) as the direction in which the potential of the signal $\overline{D_i}$ changes, while the second dissymmetric type differential amplifier circuit P_2 forms an output signal D_i' whose potential changes in the same direction (in-phase) as the direction in which the potential of the signal D_i changes. More specifically, the gates of the MISFETs Q_{202} and Q_{206} being the inverting input terminals (-) of the first and second dissymmetric type differential amplifier circuits P_1 and P_2 are respectively supplied with the signals D_i and $\overline{D_i}$. The gates of the MISFETs Q_{201} and Q_{205} being the non-inverting input terminals (+)

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are respectively supplied with the signals $\overline{D}_1$ and D_1 by the cross-connection. In consequence, the first dissymmetric type differential amplifier circuit P_1 provides the output signal $\overline{D}_1'$ whose potential changes in the same direction (in-phase) as the direction of the potential change of the signal $\overline{D}_1$, while the second dissymmetric type differential amplifier circuit P_2 provides the output signal D_1' whose potential changes in the same direction (in-phase) as the direction of the potential change of the signal D_1 . Moreover, the constituent loads of the first and second dissymmetric type differential amplifier circuits P_1 and P_2 are the active loads. Therefore, the first dissymmetric type differential amplifier circuit P_1 can form the output signal $\overline{D}_1'$ whose potential changes more than the change of the potential of the signal $\overline{D}_1$, while the second dissymmetric type differential amplifier circuit P_2 can form the output signal D_1' whose potential changes more than the change of the potential of the signal D_1 .

In this embodiment, the output signals D_1' and $\overline{D}_1'$ from the first and second dissymmetric type differential amplifier circuits P_1 and P_2 are applied to the third dissymmetric type differential amplifier circuit P_3 in order to make the voltage gain of the sense amplifier great.

An output signal OUT (D_1) from the third dissymmetric type differential amplifier circuit P_3 is transmitted to the input terminal IN of the data output buffer DCB shown in Figure 5.

5 In this embodiment, a MISFET Q_{209} is forms a constant-current source common to the first and second dissymmetric type differential amplifier circuits P_1 and P_2 . In place of the MISFET Q_{209} , MISFETs forming constant-current sources
10 may well be arranged in the respective dissymmetric type differential amplifier circuits P_1 and P_2 .

Each of the first, second and third differential amplifier circuits P_1 , P_2 and P_3 receives a pair of signals complementary to each other, and delivers
15 a single signal having a potential which corresponds to the potential difference between the complementary signals with respect to earth potential of the circuitry. That is, the differential amplifier circuit receives the two signals and delivers the single signal
20 only. As a different differential amplifier circuit, there is the type which receives two signals and which delivers two signals. In order to distinguish the differential amplifier circuit of this type from the foregoing differential amplifier circuit (for example,
25 P_1 , P_2 or P_3), the latter shall be called the "dissymmetric

type differential amplifier circuit" as stated above.

In a case where a desired sense amplifier is selected from among the plurality of sense amplifiers as in the embodiment shown in Figure 2A, the MISFETs Q_{209} and Q_{214} as the constant current sources are switched and controlled by a control circuit CONT which is constructed of an inverter circuit IV_1 receiving a control signal SAC, an inverter circuit IV_2 receiving a memory array selecting signal m_1 , and MISFETs Q_{215} to Q_{218} .

In contrast, in a case where the plurality of sense amplifiers are simultaneously operated as in the embodiment of Figure 3A, the signal CS12 as shown in Figure 3B is applied to the gates of the MISFETs Q_{209} and Q_{214} as the constant current sources.

According to this embodiment, the signals D_1' and $\overline{D_1'}$ balanced to each other are formed by the use of the two dissymmetric type differential amplifier circuits P_1 and P_2 . That is, the signals D_1' and $\overline{D_1'}$ which correspond to the signals D_1 and $\overline{D_1}$ complementary to each other and which are amplified are formed by the first and second dissymmetric type differential amplifier circuits P_1 and P_2 . More specifically, when the potential of the signal D_1' has risen by way of example, the potential of the signal $\overline{D_1'}$ falls

an amount substantially equal to the rise value of the potential of the signal D_1' . Therefore, the similar dissymmetric type differential amplifier circuit P_3 can be located at the succeeding stage in order to further raise the gain.

The first and second dissymmetric type differential amplifier circuits P_1 and P_2 can be endowed with offset voltages similar to each other by forming them within an identical monolithic IC. More specifically, in the case where the first and second dissymmetric type differential amplifier circuits P_1 and P_2 are formed on an identical semiconductor substrate, the changes of the characteristics of elements constituting the first dissymmetric type differential amplifier circuit P_1 as attributed to the variations of manufacturing conditions, etc. become similar to the changes of the characteristics of elements constituting the second dissymmetric type differential amplifier circuit P_2 . In consequence, the offset of the first dissymmetric type differential amplifier circuit ascribable to the changes of the characteristics of the constituent elements becomes substantially similar to the offset of the second dissymmetric type differential amplifier circuit also ascribable to the changes of the characteristics of the elements. It is supposed by way of example that when the input

terminals (+) and (-) of the first dissymmetric type differential amplifier circuit P_1 are supplied with a pair of input signals which render the potential difference between them zero (V), a certain positive offset voltage is provided from the dissymmetric type differential amplifier circuit P_1 on account of the offset thereof. Then, when the second dissymmetric type differential amplifier circuit P_2 is supplied with the same input signals as those of the first one P_1 , it provides on account of its offset an offset voltage similar to the offset voltage provided from the first dissymmetric type differential amplifier circuit P_1 .

Therefore, the output signals D_1' and $\overline{D_1'}$ formed by the dissymmetric type differential amplifier circuits P_1 and P_2 include the offset voltages similar to each other. The output signals D_1' and $\overline{D_1'}$ are respectively applied to the third dissymmetric type differential amplifier circuit P_3 . Because of a differential amplifier circuit, this third dissymmetric type differential amplifier circuit P_3 can cancel the offset voltage of the first dissymmetric type differential amplifier circuit P_1 included in the output signal D_1' and the offset voltage of the second dissymmetric type differential amplifier circuit P_2 included in the output signal $\overline{D_1'}$.

Accordingly, the offset voltages of the first and second dissymmetric type differential amplifier circuits P_1 and P_2 are not included in the output signal OUT (D"). An offset voltage possessed by the third dissymmetric type differential amplifier circuit P_3 is transmitted to the succeeding stage. Since, however, the signal level of the output signal OUT (D") of this dissymmetric type differential amplifier circuit P_3 is sufficiently great, the above offset voltage can be substantially neglected.

Since the offsets of the dissymmetric type differential amplifier circuits P_2 and P_1 are cancelled in the third dissymmetric type differential amplifier circuit P_3 , respectively, the MISFETs Q_{209} and Q_{214} constituting the constant sources can be simultaneously operated. Therefore, the output signal OUT (D") can be derived at high speed. Accordingly, the operation of the static RAM can be rendered fast.

Even in a case where in-phase noise has acted on the input signals D_1 and $\overline{D_1}$, it is cancelled because the circuits P_1 and P_2 are differential amplifier circuits. Accordingly, noise is not transmitted to the succeeding stage. Likewise, even in a case where in-phase noise has been involved in the output signals D_1 and $\overline{D_1}$, it is cancelled and not transmitted to the succeeding stage because the circuit P_3

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is a differential amplifier circuit.

As described above, according to this embodiment, there can be provided the sense amplifier which reduces the influences of the offset voltages possessed by the differential amplifier circuits and the noise and which exhibits a high sensibility as well as a high gain. For this reason, even when the potential difference between the signals D_i and $\overline{D_i}$ from the pair of common data lines is comparatively small, the sense amplifier can drive the data output buffer satisfactorily. Accordingly, the sense amplifier can drive the data output buffer in a short time after the pair of information complementary to each other have been delivered from the memory cell to the pair of data lines D and $\overline{D}$. It is accordingly possible to attain a high-speed operation of the static RAM. For example, even when the voltage difference of the signals D_i and $\overline{D_i}$ from the pair of common data lines CDL and $\overline{CDL}$ is as small as about 0.2 volt, the sense amplifier SA of this embodiment can form an output signal great enough to drive the data output buffer DOB, so that the operation of the static RAM can be rendered fast.

The dissymmetric type differential amplifier circuit shown in Figure 6 can be replaced with a latch circuit including a pair of MISFETs the gates and drains

of which are cross-connected to each other. In this case, however, a comparatively long time is required for releasing a status held in the latch circuit and bringing the latch circuit into the opposite status. Therefore, the operating speed of the static RAM is limited, and it cannot be made high.

In the circuit of the embodiment shown in Figure 6 the third dissymmetric type differential amplifier circuit P_3 can be omitted and the signals D_i' and $\overline{D_i'}$ can be transmitted to the data output buffer DOB of the succeeding stage. In this case, in the data output buffer DOB shown in Figure 5, the inverter circuit G_{103} is omitted, and the signals D_i' and $\overline{D_i'}$ are directly applied to the respective terminals T_1 and T_2 . Therefore, the data output buffer DOB can be simplified.

In this case, the balanced signals D_i' and $\overline{D_i'}$ are made the output signals of the sense amplifier SA. Therefore, the potential difference between the output signals of the sense amplifier SA becomes approximately double in comparison with the amplitude of the output signal of the sense amplifier which employs the single dissymmetric type differential amplifier circuit as stated before. In other words, such sense amplifier SA comes to have a gain which is approximately double

that of the prior-art sense amplifier. As stated before, this sense amplifier can cancel in-phase noise.

In this case, a static RAM of still fewer malfunctions can be provided in such a way that the balanced signals D_1' and $\overline{D_1'}$ are compared in the data output buffer and that the potential of the output signal of the data output buffer is determined to the high level or the low level on the basis of the result of the comparison. More specifically, in the case where, as described before, the high level or low level of the output signal of the sense amplifier is detected depending upon whether the potential of the output signal from the sense amplifier is higher or lower than the logic threshold voltage of the data output buffer with respect to earth potential of the circuitry, the noise margin of the data output buffer becomes small due to the variation of the logic threshold voltage attributed to the variations of the manufacturing conditions. In contrast, the comparison between the balanced signals D_1' and $\overline{D_1'}$ is the comparison between the relative potentials of the two signals, and it is less susceptible to the variations of the manufacturing conditions unlike the comparison between the output signal of the sense amplifier and the reference voltage (threshold voltage) whose value varies depending upon

the manufacturing conditions as stated above. Accordingly, the static RAM of still fewer malfunctions can be provided.

Figure 7 shows a block diagram of another embodiment of this invention.

In this embodiment, the balanced signals D_1' and $\overline{D_1'}$ are formed by dissymmetric type differential amplifier circuits P_1 and P_2 similar to the foregoing. Balanced output signals OUT and $\overline{OUT}$ are formed by arranging similarly dissymmetric type differential amplifier circuits P_4 and P_5 . Since the practicable circuits of the respective dissymmetric type differential amplifier circuits P_1 , P_2 and P_4 , P_5 are similar to those in Figure 6, they are not explained further.

In the case of supplying the balanced output signals OUT and $\overline{OUT}$ to the data output buffer DOB shown in Figure 5, the inverter circuit G_{103} in this data output buffer DOB is omitted, and the output signals OUT and $\overline{OUT}$ are directly applied to the one-side input terminals T_1 and T_2 of the respective gate circuits G_{101} and G_{102} . Accordingly, the data output buffer DOB can be simplified. In this embodiment, the balanced signals OUT and $\overline{OUT}$ are made the output signals of the sense amplifier. Therefore, the potential difference between the output signals of this sense amplifier becomes approximately

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double the amplitude of the output signal OUT of the sense amplifier shown in Figure 5. In other words, the sense amplifier of this embodiment has a gain which is approximately double that of the sense amplifier SA shown in Figure 6.

Also in this embodiment, by forming the dissymmetric type differential amplifiers P_1 and P_2 on an identical semiconductor substrate, offset voltages possessed by the dissymmetric type differential amplifier circuits P_1 and P_2 are cancelled in the dissymmetric type differential amplifier circuits P_4 and P_5 for the same reason as explained in connection with Figure 6. Accordingly, the offset voltages of the dissymmetric type differential amplifier circuits P_1 and P_2 are not included in the output signals OUT and $\overline{\text{OUT}}$. The offset voltages of the dissymmetric type differential amplifier circuits P_4 and P_5 are respectively included in the output signals OUT and $\overline{\text{OUT}}$. Since, however, the potential difference between the output signals OUT and $\overline{\text{OUT}}$ is sufficiently greater than the offset voltages, these offset voltages are substantially negligible.

In the case where in-phase noise has been involved in the signals D_1 and $\overline{D_1}$, it is cancelled in the dissymmetric type differential amplifier circuits P_1 and P_2 . Similarly, in the case where in-phase noise has been involved in the signals

D_1' and $\overline{D_1'}$, it is cancelled in the dissymmetric type differential amplifier circuits P_4 and P_5 . Accordingly, even when the in-phase noise has acted on the signals D_1 , $\overline{D_1}$ or (and) the signals D_1' , $\overline{D_1'}$, the respective potentials of the output signals OUT and $\overline{OUT}$ are not changed by the noise.

As described above, according to this embodiment, there can be provided a sense amplifier which reduces the influences of the offset voltages and the noise still more and which has a high sensibility as well as a high gain.

Figure 8 is a circuit diagram showing another practicable embodiment of the dissymmetric type differential amplifier circuit P.

In this embodiment, the dissymmetric type differential amplifier circuit is constructed of a pair of MISFETs Q_{219} and Q_{220} which are connected in the differential mode, a MISFET Q_{221} whose gate is earthed and which serves as the load of the MISFET Q_{219} , and a MISFET Q_{222} whose gate has the common drain of the MISFETs Q_{219} and Q_{221} connected thereto. The dissymmetric type differential amplifier circuit P of this embodiment has a higher gain in comparison with a dissymmetric type differential amplifier circuit employing a current mirror circuit as its load, for example, the dissymmetric

type differential amplifier circuit P₁ shown in Figure 6.

On the other hand, however, it has a comparatively great offset voltage. More specifically, in the dissymmetric type differential amplifier P, the MISFET Q₂₂₁ operates as the load having a comparatively great resistance.

It is therefore permitted to apply a comparatively great voltage between the gate and source of the MISFET Q₂₂₂. In consequence, this dissymmetric type differential

amplifier P has a high gain. However, the characteristics of the MISFET Q₂₁₉ and those of the MISFET Q₂₂₀ disagree on account of, for example, the variations of the manufacturing conditions. In a case where, in spite

of input signals of equal potentials applied to a non-inverting input terminal (+) and an inverting input

terminal (-), the drain current of the MISFET Q₂₁₉ has become higher than that of the MISFET Q₂₂₀, a comparatively great voltage is applied between the gate and source of the MISFET Q₂₂₂ because the MISFET Q₂₂₁ is the load having the comparatively great resistance.

Therefore, the mutual conductance of the MISFET Q₂₂₂ becomes high, and a current of high value is provided. That is, the dissymmetric type differential amplifier circuit P has the comparatively great offset voltage.

However, in a case where the dissymmetric type differential amplifier circuit as shown in Figure 8 is used for the

dissymmetric type differential amplifier circuits P_1 and P_2 in Figure 6 or 7, the offset voltages are cancelled. Therefore, the offset voltage poses no problem, and the high gain is exploited.

5 Figure 9 shows a layout diagram (plan view) in the case where the dissymmetric type differential amplifier circuits P_1 and P_2 in Figure 6 or 7 are formed on a monolithic IC.

10 In Figure 9, parts enclosed with thick solid lines indicate aluminium wiring layers. The aluminium wiring layers are used as the wiring layer of the supply voltage V_{cc} , the wiring layer of earth potential GND of the circuitry, a wiring layer for connecting the respective source layers of the differential MISFETs Q_{201} , Q_{202} and Q_{205} , Q_{206} in common, and a
15 wiring layer for connecting the drain layer of the differential MISFET and the drain layer of the load MISFET.

20 In the figure, parts enclosed with thin solid lines indicate conductive polycrystalline silicon layers. The conductive polycrystalline silicon layers are used for the gate electrodes of the respective MISFETs and wiring layers associated therewith,

25 Parts enclosed with broken lines indicate p-type or n-type diffused layers. The diffused layers are used

as the source layer or drain layer of the MISFET and a wiring layer for connecting the gate of the differential MISFET.

A part enclosed with a dot-and-dash line
5 indicates a p-type well layer formed on an n-type substrate. Accordingly, the n-channel MISFETs are formed in the P-wall. Marks ☒ indicate contacts.

The system arrangement of the static type RAM can adopt various aspects of performance.

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CLAIMS.

1. A static type semiconductor random access memory including: memory cells each of which delivers a pair of signals complementary to each other; a first dissymmetric type differential amplifier circuit whose non-inverting input terminal is supplied with one signal of the pair of complementary signals, whose inverting input terminal is supplied with the other signal of the pair of complementary signals and which forms a first output signal in-phase with the signal supplied to the non-inverting input terminal; a second dissymmetric type differential amplifier circuit whose inverting input terminal is supplied with said one signal, whose non-inverting input terminal is supplied with the other signal and which forms a second output signal in-phase with said signal supplied to said non-inverting input terminal; and first means supplied with the first output signal and the second output signal for forming a third output signal based on the first output signal and said second output signal.

2. A static type semiconductor random access memory according to Claim 1, wherein said first means comprises a third dissymmetric type differential amplifier circuit whose non-inverting input terminal is supplied with the first output



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signal, whose inverting input terminal is supplied with the second output signal and which forms a fourth output signal in-phase with the signal supplied to said non-inverting input terminal; and wherein second means is provided to receive the fourth output signal and to form the third output signal.

3. A static type semiconductor random access memory according to Claim 1, wherein the said first means comprises a fourth dissymmetric type differential amplifier circuit whose non-inverting input terminal is supplied with the first output signal, whose inverting input terminal is supplied with the second output signal and which forms a fifth output signal in-phase with the signal supplied to said non-inverting input terminal; a fifth dissymmetric type differential amplifier circuit whose inverting input terminal is supplied with the first output signal, whose non-inverting input terminal is supplied with the second output signal and which forms a sixth output signal in-phase with the signal supplied to said non-inverting input terminal; and wherein third means is provided to receive the fifth output signal and the sixth output signal and to form the third output signal.



4. A static type semiconductor random access memory according to Claim 1, wherein each of said first and second dissymmetric type differential amplifier circuits is a dissymmetric type differential amplifier which comprises a first insulated-gate field effect transistor of a first conductivity type having its gate coupled to the non-inverting input terminal, a second insulated-gate field effect transistor of said first conductivity type having its gate coupled to the inverting input terminal and having its source coupled to the source of the first insulated-gate field effect transistor, and first active load means coupled to respective drains of the first and second insulated-gate field effect transistors, and in which the signal in-phase with the signal supplied to the non-inverting input terminal is derived from the drain of the second insulated-gate field effect transistor.

5. A static type semiconductor random access memory according to Claim 2, wherein each of said first and second dissymmetric type differential amplifier circuits is a dissymmetric type differential amplifier which comprises a third insulated-gate field effect transistor of the first conductivity type having its gate coupled to the non-inverting input terminal, a fourth insulated-gate field effect transistor of the first conductivity type having its



gate coupled to the inverting input terminal and having its source coupled to the source of the third insulated-gate field effect transistor, and second active load means coupled to respective drains of the third and fourth insulated gate field effect transistors, and in which the signal in-phase with the signal supplied to said non-inverting input terminal is derived from the drain of the fourth insulated-gate field effect transistor; and wherein said third dissymmetric type differential amplifier circuit is a dissymmetric type differential amplifier circuit which comprises a first insulated-gate field effect transistor of the first conductivity type having its gate coupled to the non-inverting input terminal, a second insulated-gate field effect transistor of the first conductivity type having its gate coupled to the inverting input terminal and having its source coupled to the source of the first insulated-gate field effect transistor, and first active load means coupled to respective drains of the first and second insulated-gate field effect transistors, and in which the signal in-phase with the signal supplied to the non-inverting input terminal is derived from the drain of said second insulated-gate field effect transistor.



6. A static type semiconductor random access memory according to Claim 3, wherein each of the said first and second dissymmetric type differential amplifier circuits is a dissymmetric type differential amplifier which comprises a third insulated-gate field effect transistor of the first conductivity type having its gate coupled to the non-inverting input terminal, a fourth insulated-gate field effect transistor of the first conductivity type having its gate coupled to the inverting input terminal and having its source coupled to the source of the third insulated-gate field effect transistor, and second active load means coupled to respective drains of the third and fourth insulated-gate field effect transistors, and in which the signal in-phase with the signal supplied to the non-inverting input terminal is derived from the drain of the fourth insulated-gate field effect transistor; and wherein each of said fourth and fifth dissymmetric type differential amplifier circuits is a dissymmetric type differential amplifier circuit which comprises a first insulated-gate field effect transistor of the first conductivity type having its gate coupled to the non-inverting input terminal, a second insulated-gate field effect transistor of the first conductivity type having its gate coupled to the inverting input terminal and having its source coupled to the source of the first insulated-gate field effect transistor, and first active



load means coupled to respective drains of the first and second insulated-gate field effect transistors, and in which the signal in-phase with the signal supplied to the non-inverting input terminal is derived from the drain of the second insulated-gate field effect transistor.

7. A static type semiconductor random access memory according to Claim 4, wherein said first active load means comprises a fifth insulated-gate field effect transistor of a second conductivity type whose drain is coupled to the drain of the second insulated-gate field effect transistor and whose gate is coupled to the drain of the first insulated-gate field effect transistor, and first load means coupled between the gate and a source of the fifth insulated-gate field effect transistor.

8. A static type semiconductor random access memory according to Claim 5 or Claim 6, wherein said first active load means comprises a fifth insulated-gate field effect transistor of a second conductivity type whose drain is coupled to the drain of the second insulated-gate field effect transistor and whose gate is coupled to the drain of the first insulated-gate field effect transistor, and first load means coupled between the gate and a source of the fifth insulated-gate field effect transistor, and wherein the second active load means comprises a sixth insulated-gate



field effect transistor of the second conductivity type whose drain is coupled to the drain of the fourth insulated-gate field effect transistor and whose gate is coupled to the drain of the third insulated-gate field effect transistor, and second load means coupled between the gate and a source of the sixth insulated-gate field effect transistor.

9. A static type semiconductor random access memory according to Claim 7, wherein said first load means comprises a seventh insulated-gate field effect transistor of the second conductivity type whose source is connected to the source of the fifth insulated-gate field effect transistor and whose gate and drain are coupled to the gate of the fifth insulated-gate field effect transistor.

10. A static type semiconductor random access memory according to Claim 8, wherein said first load means comprises a seventh insulated-gate field effect transistor of the second conductivity type whose source is coupled to the source of the fifth insulated-gate field effect transistor and whose gate and drain are coupled to the gate of the fifth insulated-gate field effect transistor, and wherein said second load means comprises an eighth insulated-gate field effect transistor of the second conductivity type whose source is coupled to the source of the sixth insulated-gate field effect transistor and whose gate and drain are coupled to the gate of the sixth insulated-gate field effect transistor.



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11. A static type semiconductor random access memory according to Claim 8, wherein said second load means includes a ninth insulated-gate field effect transistor of the second conductivity type whose source is coupled to the source of the sixth insulated-gate field effect transistor, whose drain is coupled to the drain of said third insulated-gate field effect transistor and whose gate is coupled to earth.

12. A static type semiconductor random access memory constructed and arranged to operate substantially as herein described with reference to and as illustrated in the accompanying drawings.

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