

CLAIMS

1. A data reading method, comprising:

determining whether a preset cache area has cached data that a read target address points to when receiving a read instruction that comprises the read target address; and

5 finding a cache address corresponding to the read target address according to a first mapping relationship if the preset cache area has cached the data that the read target address points to, and reading, from the preset cache area, data that the cache address points to, wherein the first mapping relationship is used to record a correspondence between the read target address and the cache address; and

10 reading, from non-volatile storage space, the data that the read target address points to if the preset cache area has not cached the data that the read target address points to;;

when receiving a write instruction, determining whether a write target address in the write instruction belongs to a most significant bit page MSB page in the non-volatile storage space, wherein the write instruction comprises to be written data and the write target address; and

15 if the write target address does not belong to an MSB page in the non-volatile storage space, storing, in the preset cache area and the non-volatile storage space that is corresponding to the write target address, the to be written data, and establishing the first mapping relationship between the cache address and the write target address; or if the write target address belongs to an MSB page in the non-volatile storage space, storing, in the non-volatile storage space corresponding to the write
20 target address, the to be written data.

2. The method according to claim 2, further comprising:

obtaining a maximum page number difference m between an MSB page and an LSB page in all groups of shared pages in the non-volatile storage space, wherein m is a natural number; and

25 allocating cache space with a size of at least $n \cdot p + m$ pages for the preset cache area, wherein p represents a quantity of shared pages of an MSB page in the non-volatile storage space, and n is a natural number and is at least 1.

3. The method according to claim 2, further comprising:

30 if the write target address belongs to an MSB page in the non-volatile storage space, determining whether the MSB page in which the write target address is located is the last MSB page in a block;

if the MSB page in which the write target address is located is not the last MSB page in the block, obtaining an address of a shared page of the n^{th} MSB page as counted forward from the MSB page in which the write target address is located, and using the obtained address as a data release

address; or if the MSB page in which the write target address is located is the last MSB page in the block, obtaining addresses of shared pages of the last $n+1$ MSB pages in the block, and using the obtained addresses as a data release addresses; and

releasing data that is in the preset cache area and a cache address having the first mapping relationship with the data release address points to, and deleting the data release address from the first mapping relationship.

4. The method according to any one of claims 1 to 3, further comprising:

during power-off, saving data that is in the preset cache area in the non-volatile storage space, and establishing a second mapping relationship between the cache address and a save address that is in the non-volatile storage space; and

during power-on, caching, at the cache address in the preset cache area according to the second mapping relationship, the data that the save address in the non-volatile storage space points to.

5. The method according to any one of claims 1 to 3, wherein the preset cache area is located in a double data rate synchronous dynamic random access memory, DDR SDRAM or a static random access memory SRAM.

6. The method according to any one of claims 1 to 3, wherein the non-volatile storage space is storage space of a solid state drive SSD.

7. A data reading apparatus, comprising a first determining module, a first reading module, and a second reading module, wherein

the first determining module is configured to: when receiving a read instruction that comprises a read target address, determine whether a preset cache area has cached data that the read target address points to, and send a first determining result to the first and second reading modules;

the first reading module is configured to: when the preset cache area has cached the data that the read target address points to, find a cache address corresponding to the read target address according to a first mapping relationship, and read, from the preset cache area, data that the cache address points to, wherein the first mapping relationship is used to record a correspondence between the target address and the cache address; and

the second reading module is configured to: when the preset cache area has not cached the data that the read target address points to, read, from a non-volatile storage space, the data that the read target address points to;

wherein the apparatus further comprises a second determining module, a first writing module, and a second writing module, wherein

the second determining module is configured to: when receiving a write instruction, determine whether a write target address in the write instruction belongs to a most significant bit page MSB

page in the non-volatile storage space, and send a second determining result to the first and second writing modules, wherein the write instruction comprises to be written data and the write target address;

the first writing module is configured to: when it is determined that the write target address does not belong to an MSB page in the non-volatile storage space, store, in the preset cache area and the non-volatile storage space that is corresponding to the write target address, the to be written data, and establish the first mapping relationship between the cache address and the write target address; and

the second writing module is configured to: when it is determined that the write target address belongs to an MSB page in the non-volatile storage space, store, in the non-volatile storage space corresponding to the write target address, the to be written data.

8. The apparatus according to claim 7, further comprising a third obtaining module and an allocating module, wherein

the third obtaining module is configured to obtain a maximum page number difference m between an MSB page and an LSB page in all groups of shared pages in the non-volatile storage space, and send m to the allocating module, wherein m is a natural number; and

the allocating module is configured to allocate cache space with a size of at least $n \cdot p + m$ pages for the preset cache area, wherein p represents a quantity of shared pages of an MSB page in the non-volatile storage space, and n is a natural number and is at least 1.

9. The apparatus according to claim 8, further comprising a third determining module, a first obtaining module, a second obtaining module, and a releasing module, wherein

the third determining module is configured to: when the write target address belongs to an MSB page in the non-volatile storage space, determine whether the MSB page in which the write target address is located is the last MSB page in a block, and send a third determining result to the first and second obtaining modules;

the first obtaining module is configured to: when the MSB page in which the write target address is located is not the last MSB page in the block, obtain an address of a shared page of the n^{th} MSB page as counted forward from the MSB page in which the write target address is located, use the obtained address as a data release address, and send the data release address to the releasing module;

the second obtaining module is configured to: when the MSB page in which the write target address is located is the last MSB page in the block, obtain addresses of shared pages of the last $n+1$ MSB pages in the block, use the obtained addresses as the data release addresses, and send the data release addresses to the releasing module; and

the releasing module is configured to release data that is in the preset cache area and that a cache address having the first mapping relationship with the data release address points to, and delete the data release address from the first mapping relationship.

10. The apparatus according to any one of claims 7 to 9, further comprising a saving module
5 and a caching module, wherein

the saving module is configured to: during power-off, save data that is in the preset cache area in the non-volatile storage space, establish a second mapping relationship between the cache address and a save address that is in the non-volatile storage space, and send the second mapping relationship to the caching module; and

10 the caching module is configured to: during power-on, cache, at the cache address in the preset cache area according to the second mapping relationship, the data that the save address in the non-volatile storage space points to.

11. The apparatus according to claim 7, wherein the preset cache area is located in a double data rate synchronous dynamic random access memory DDR or a static random access memory
15 SRAM.

12. The apparatus according to claim 7, wherein the non-volatile storage space is storage space of a solid state drive SSD.