Claims

What is claimed:

1. A semiconductor device, comprising:

a substrate;

a vertical interconnect structure formed in contact with a first surface of the substrate, wherein the substrate includes an opening extending from a second surface of the substrate opposite the first surface of the substrate to the vertical interconnect structure;

a semiconductor die disposed over the first surface of the substrate;

an encapsulant deposited over the first surface of the substrate, a side surface of the substrate, and around the semiconductor die, including a surface of the encapsulant outside the substrate coplanar with the second surface of the substrate; and

a first interconnect structure formed over the encapsulant opposite the substrate and coupled to the semiconductor die.

2. The semiconductor device of claim 1, wherein the substrate includes:

a first conductive layer formed over first surface of the substrate;

a second conductive layer formed over the second surface of the substrate; and

a conductive via formed through the substrate and contacting the first conductive layer and second conductive layer.

3. The semiconductor device of claim 2, further including:

a first insulating layer formed over the first surface of the substrate; and

a second insulating layer formed over the second surface of the substrate.

4. The semiconductor device of claim 1, wherein a portion of the vertical interconnect structure extends out from the encapsulant.

5. The semiconductor device of claim 1, wherein the vertical interconnect structure includes a plurality of bumps.

6. The semiconductor device of claim 1, further including a semiconductor package disposed over the substrate and electrically connected to the substrate.

7. The semiconductor device of claim 1, wherein a surface of the semiconductor die opposite an active surface of the semiconductor die is devoid of the encapsulant.

8. The semiconductor device of claim 1, wherein the second surface of the substrate is planarized.

9. A semiconductor device, comprising:

a substrate including,

(a) a core material,

(b) a first conductive layer formed over a first surface of the core material,

(c) a second conductive layer formed over a second surface of the core material opposite the first surface, and

(d) a conductive via formed through the core material and contacting the first conductive layer and second conductive layer;

a bump formed over the first conductive layer;

a semiconductor die disposed over a first surface of the substrate and first conductive layer;

an encapsulant deposited over the substrate and around the semiconductor die including a surface of the encapsulant outside the substrate coplanar with a second surface of the substrate opposite the first surface of the substrate; and

a first interconnect structure formed over the encapsulant opposite the substrate and coupled to the semiconductor die.

10. The semiconductor device of claim 9, wherein the substrate includes an opening extending from the second surface of the substrate to the bump.

11. The semiconductor device of claim 9, wherein the substrate further includes:

a first insulating layer formed over the first surface of the core material; and

a second insulating layer formed over the second surface of the core material.

12. The semiconductor device of claim 9, further including a semiconductor package disposed over the substrate and electrically connected to the substrate.

13. The semiconductor device of claim 9, wherein a surface of the semiconductor die opposite an active surface of the semiconductor die is devoid of the encapsulant.

14. The semiconductor device of claim 9, wherein a surface of the encapsulant is planarized.

15. A semiconductor device, comprising:

a substrate including a first interconnect structure disposed within the substrate;

a bump formed over a first surface of the substrate;

a semiconductor die disposed over the first surface of the substrate;

an encapsulant deposited over the first surface of the substrate and around the substrate including a surface of the encapsulant outside the substrate coplanar with a second surface of the substrate opposite the first surface; and

a second interconnect structure formed over and coupled to the semiconductor die opposite the substrate.

16. The semiconductor device of claim 15, wherein the bump contacts the first interconnect structure and second interconnect structure.

17. The semiconductor device of claim 15, wherein the substrate includes an opening extending from the second surface of the substrate to the bump.

18. The semiconductor device of claim 15, wherein the first interconnect structure includes:

a first conductive layer formed over the first surface of the substrate;

a second conductive layer formed over the second surface of the substrate; and

a conductive via formed through the substrate and contacting the first conductive layer and second conductive layer.

19. The semiconductor device of claim 18, further including:

a first insulating layer formed over the first surface of the substrate; and

a second insulating layer formed over the second surface of the substrate.

20. The semiconductor device of claim 15, further including a semiconductor package disposed over the substrate.

21. The semiconductor device of claim 15, wherein the second surface of the substrate is planarized.

22. The semiconductor device of claim 15, wherein the encapsulant is disposed over a side surface of the substrate.

23. The semiconductor device of claim 15, wherein a surface of the semiconductor die opposite an active surface of the semiconductor die is devoid of the encapsulant.