CLAIMS

What is claimed is:

1. A filtering system for processing an input signal, comprising:

an input interface operable to receive the input signal in a bitstream;

a filtering module operable to process the input signal through a parallel circuit of filters, wherein the processing is performed using a single sample rate; and

an output interface operable to generate an output signal based on the processed input signal.

2. The filtering system of claim 1, wherein the input signal is a multi-channel audio signal.

3. The filtering system of claim 1, wherein the input signal is a single bit digital signal.

4. The filtering system of claim 3, wherein the input signal is at multiple times the sample rate of the output signal.

5. The filtering system of claim 1, wherein the filtering system is a decimation filter system for a digital microphone.

6. The filtering system of claim 1, wherein the parallel circuit of filters comprises of a FIR filter in series with an IIR filter in each of the two paths of the parallel circuit of filters.

7. The filtering system of claim 6, wherein the FIR filter comprises of addition operations and no multiplier operations, and wherein the parallel circuit of filters utilizes a single accumulator.

8. The filtering system of claim 6, wherein one of the paths of the parallel circuit of filters is in series with a delay module in the input interface.

9. The filtering system of claim 1, wherein the parallel circuit of filters processes the input signal such that a last octave of out-of band noise remains in the processed input signal.

10. The filtering system of claim 9, wherein the output interface generates the output signal such that the last octave of out-of band noise is removed from the processed input signal.

11. The filtering system of claim 10, wherein the output interface is operable to perform an addition operation on the processed input signal from each of the two paths of the parallel circuit.

12. A method for processing an input signal with a filtering system, comprising:

receiving the input signal in a bitstream;

processing the input signal through a parallel circuit of filters, wherein the processing is performed using a single sample rate; and

generating from the filtering system an output signal based on the processed input signal.

13. The method of claim 12, wherein the input signal is a multi-channel audio signal.

14. The method of claim 12, wherein the input signal is a single bit digital signal.

15. The method of claim 12, wherein the parallel circuit of filters comprises of a FIR filter in series with an IIR filter in each of the two paths of the parallel circuit of filters.

16. The method of claim 15, wherein the FIR filter comprises of addition operations and no multiplier operations.

17. The method of claim 15, wherein one of the paths of the parallel circuit of filters is in series with a delay module in the input interface.

18. The method of claim 12, wherein processing the input signal through the parallel circuit of filters comprises leaving a last octave of out-of band noise in the processed input signal.

19. The method of claim 18, wherein generating the output signal comprises removing the last octave of out-of band noise from the processed input signal.

20. The method of claim 19, wherein generating the output signal comprises performing an addition operation on the processed input signal from each of the two paths of the parallel circuit.

CLAIMS:

1. A decimation filtering system for processing an input signal, comprising:

an input interface operable to receive the input signal in a bitstream;

a filtering module operable to process the input signal through a parallel circuit of filters comprising two paths, wherein the parallel circuit of filters comprises of a FIR filter in series with an IIR filter in each of the two paths of the parallel circuit of filters; and

an output interface operable to generate an output signal based on the processed input signal, wherein the FIR filter and IIR filter in each of the two paths process the input signal and the output interface generates the output signal at an identical sample rate.

2. The filtering system of claim 1, wherein the input signal is an audio signal.

3. The filtering system of claim 1, wherein the input signal is a single bit digital signal.

4. The filtering system of claim 1, wherein the filtering system is a digital microphone decimation filter architecture system.

5. The filtering system of claim 1, wherein the FIR filter comprises of addition operations and no multiplier operations, and wherein the parallel circuit of filters utilizes a single accumulator.

6. The filtering system of claim 1, wherein one of the paths of the parallel circuit of filters is in series with a delay module in the input interface.

7. The filtering system of claim 1, wherein the parallel circuit of filters processes the input signal such that a last octave of out-of band noise remains in the processed input signal.

8. The filtering system of claim 7, wherein the output interface generates the output signal such that the last octave of out-of band noise is removed from the processed input signal.

9. The filtering system of claim 8, wherein the output interface is operable to perform an addition operation on the processed input signal from each of the two paths of the parallel circuit.

10. A method for processing an input signal with a decimation filtering system, comprising:

receiving the input signal in a bitstream;

processing the input signal through a parallel circuit of filters, wherein the parallel circuit of filters comprises of a FIR filter in series with an IIR filter in each of the two paths of the parallel circuit of filters; and

generating an output signal based on the processed input signal, wherein processing the input signal through the parallel circuit of filters and generating the output signal are performed at an identical sample rate.

11. The method of claim 10, wherein the input signal is an audio signal.

12. The method of claim 10, wherein the input signal is a single bit digital signal.

13. The method of claim 10, wherein the FIR filter comprises of addition operations and no multiplier operations.

14. The method of claim 10, wherein one of the paths of the parallel circuit of filters is in series with a delay module in the input interface.

15. The method of claim 10, wherein processing the input signal through the parallel circuit of filters comprises leaving a last octave of out-of band noise in the processed input signal.

16. The method of claim 15, wherein generating the output signal comprises removing the last octave of out-of band noise from the processed input signal.

17. The method of claim 16, wherein generating the output signal comprises performing an addition operation on the processed input signal from each of the two paths of the parallel circuit.

18. The filtering system of claim 1, wherein the IIR filter is an Allpass Filter.

19. The filtering system of claim 18, wherein the Allpass Filter comprises a series of allpass stages.