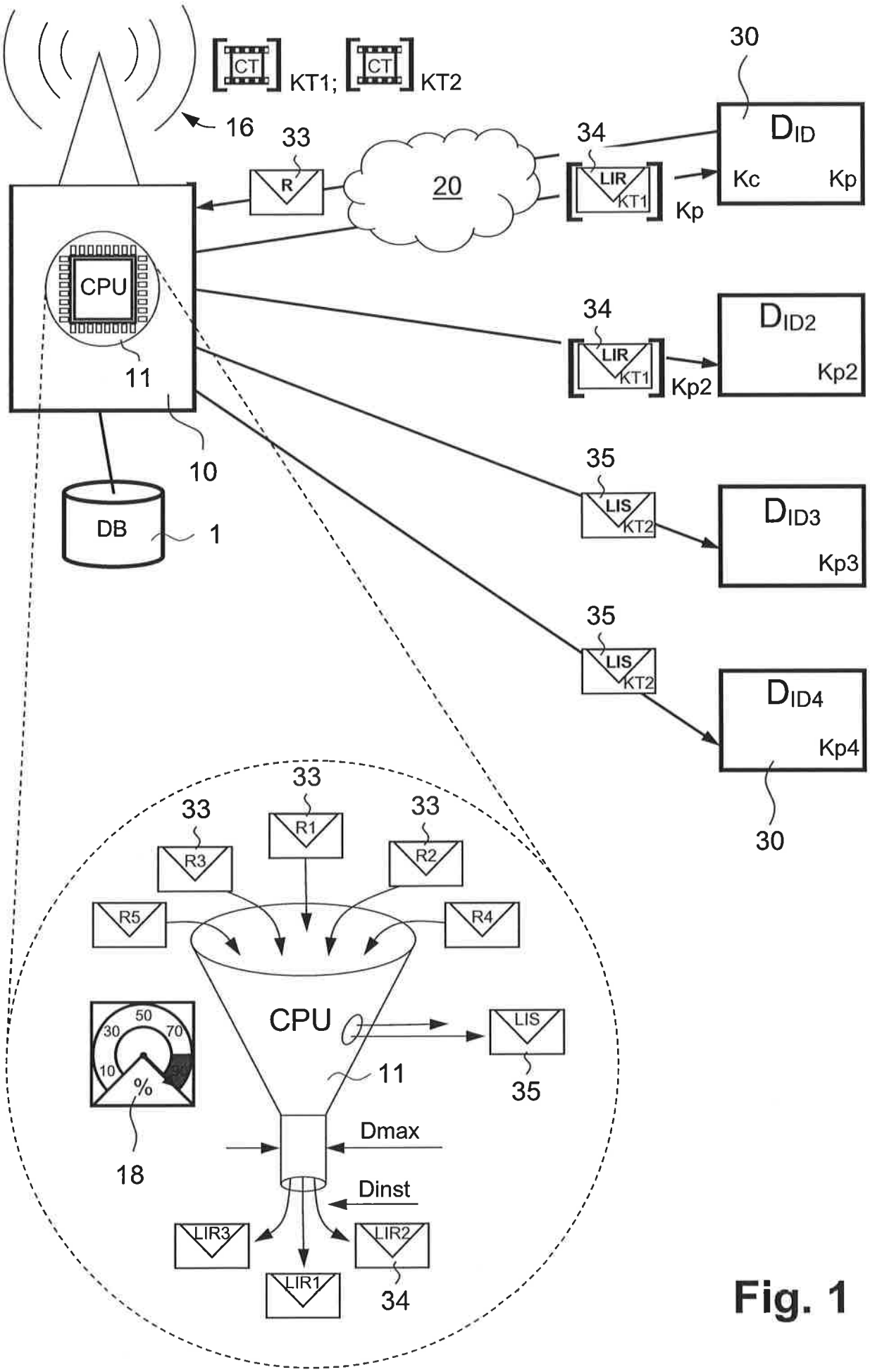
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KT1;
CT
KT2
16
33
R
20
34
LIR
KT1
Kp
30
DID
Kc
Kp
CPU
11
34
LIR
KT1
Kp2
DID2
Kp2
10
35
LIS
KT2
DID3
Kp3
DB
1
35
LIS
KT2
DID4
Kp4
30
33
R1
33
R3
33
R2
R5
R4
CPU
LIS
50
30
70
10
%
11
35
Dmax
18
Dinst
LIR3
LIR2
LIR1
34

Fig. 1

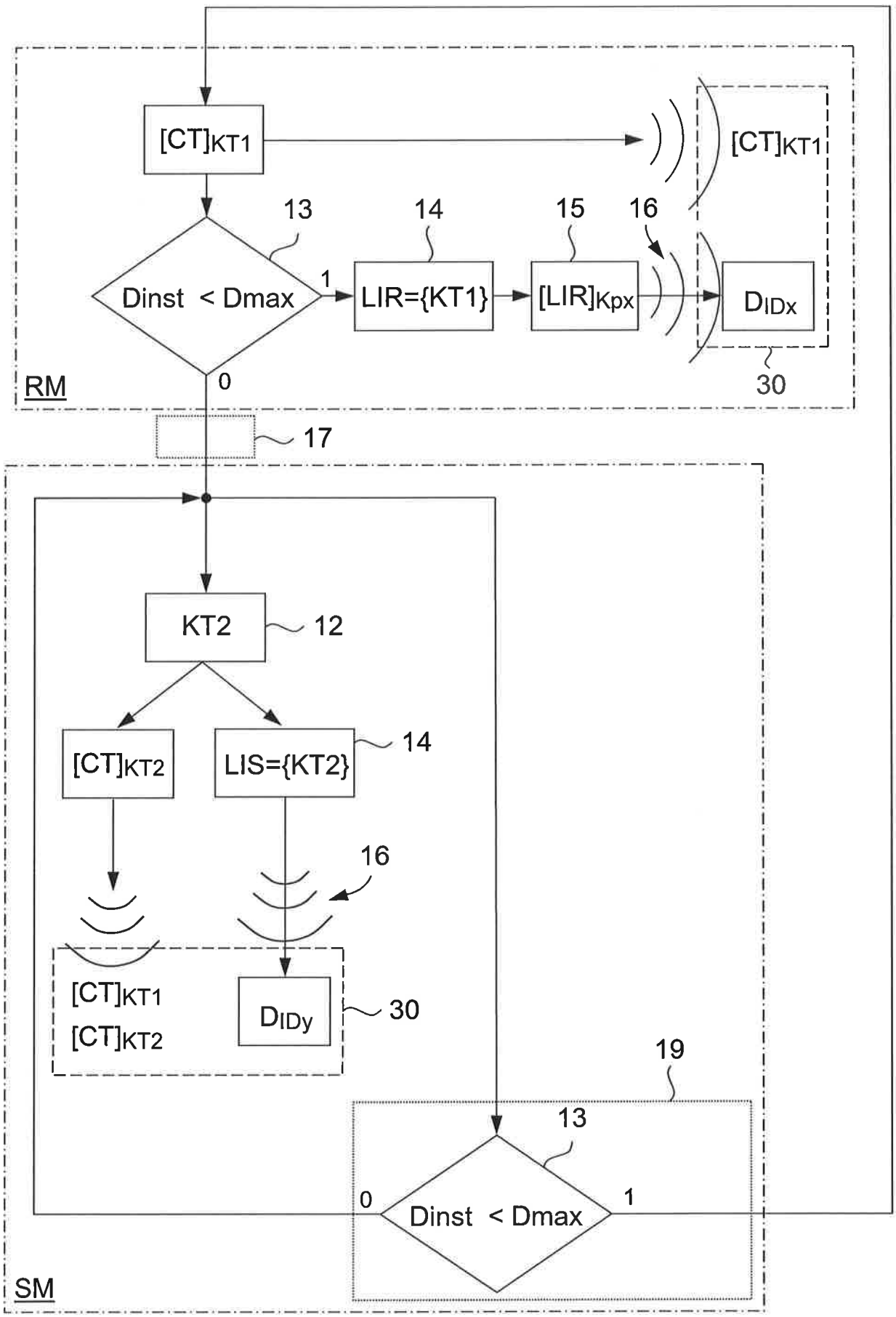
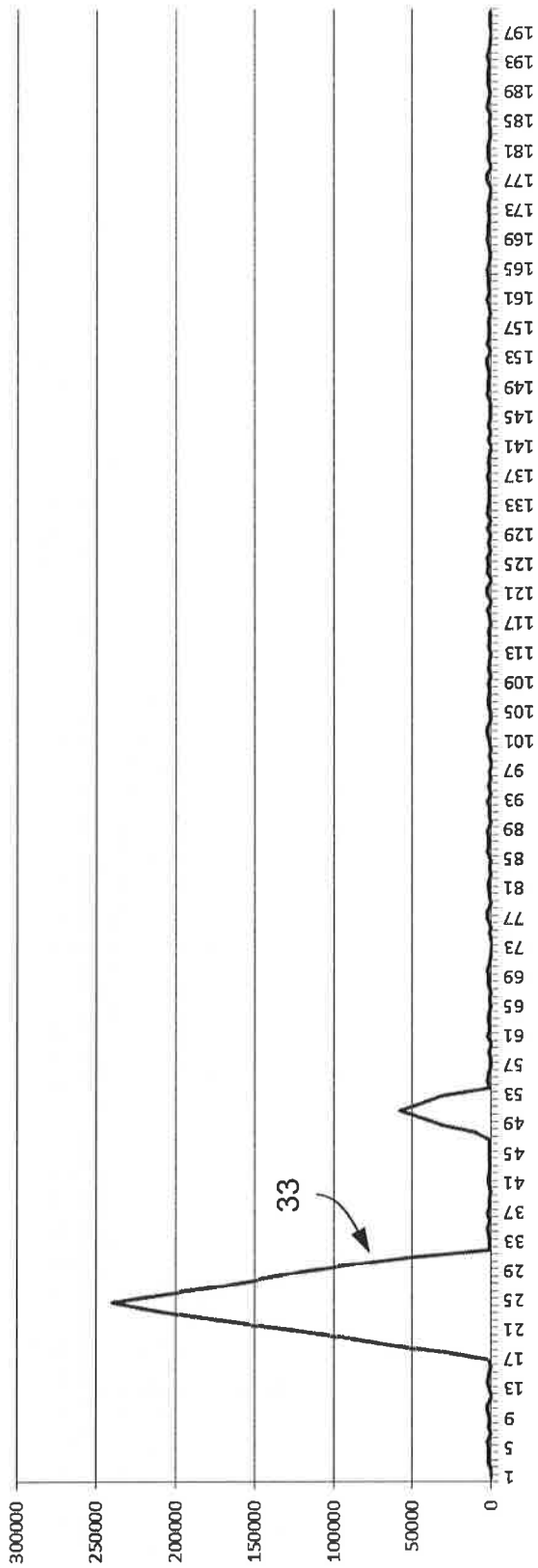

[CT]KT1
[CT]KT1
13
14
15
16
Dinst < Dmax
1
LIR={KT1}
[LIR]Kpx
DIDx
0
30
RM
17
KT2
12
[CT]KT2
LIS={KT2}
14
16
[CT]KT1
[CT]KT2
DIDy
30
19
13
0
Dinst < Dmax
1
SM

Fig. 2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200000
150000
100000
50000
0
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5
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13
17
21
25
29
33
37
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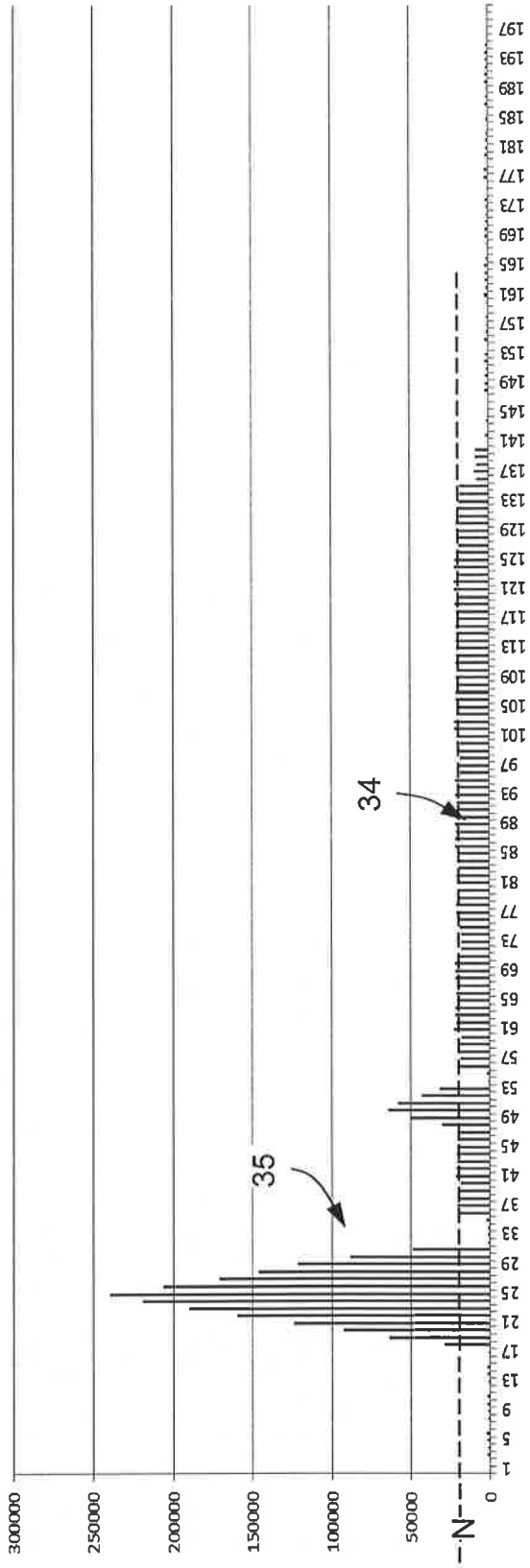
73
77
81
85
89
93
97
101
105
109
113
117
121
125
129
133
137
141
145
149
153
157
161
165
169
173
177
181
185
189
193
197
33

Fig. 3a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250000
200000
150000
100000
50000
0
1
5
9
13
17
21
25
29
33
37
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53
57
61
65
69
73
77
81
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97
101
105
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113
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121
125
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133
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161
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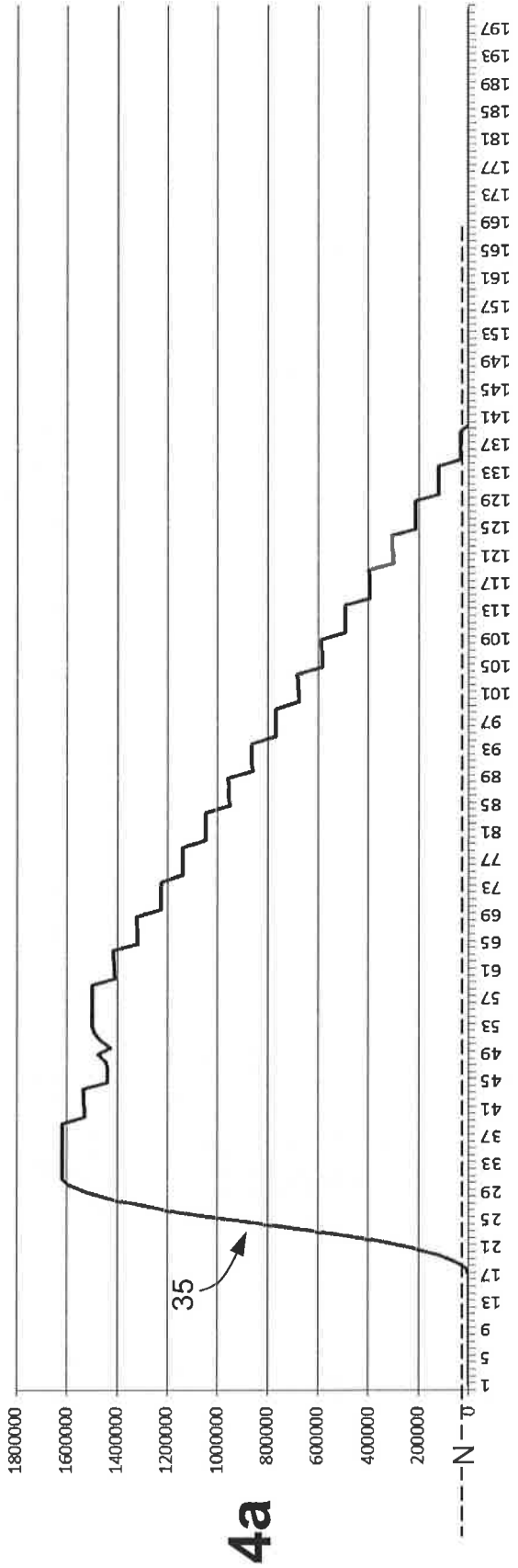
169
173
177
181
185
189
193
197
34
35
N

Fig. 3b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600000
400000
200000
0
N
35
1
5
9
13
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53
57
61
65
69
73
77
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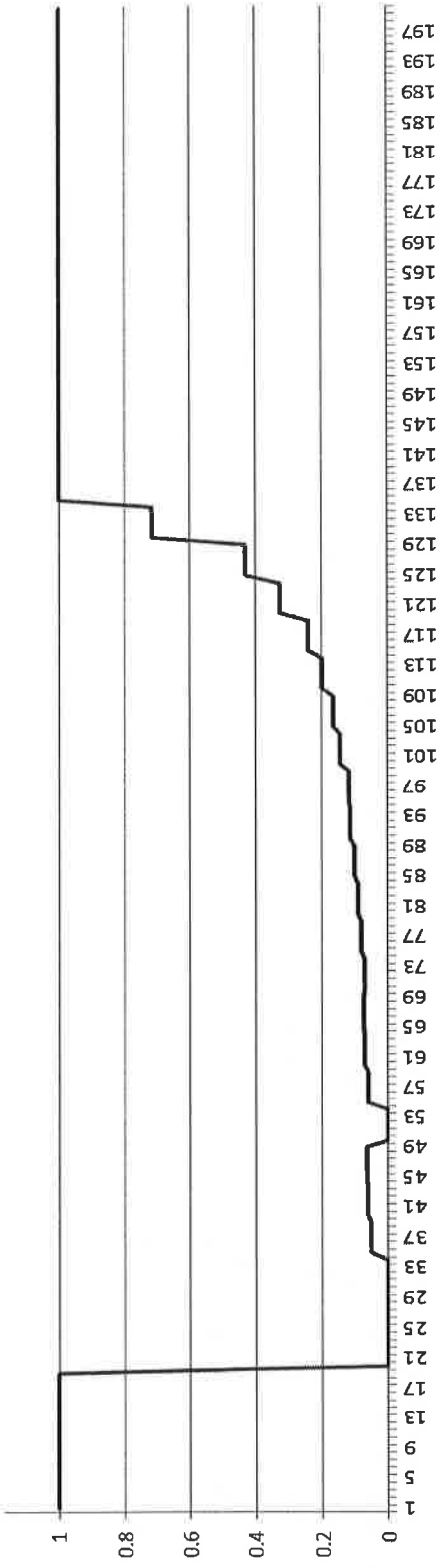
185
189
193
197

Fig. 4a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0.4
0.2
0
1
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29
33
37
41
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49
53
57
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Fig. 4b