SUMMARY

[0003a] According to a first aspect, a method of fabricating an emitter region of a solar cell is provided, the method comprising:
forming a silicon layer above a substrate;
implanting, through a stencil mask, dopant impurity atoms in the silicon layer to form implanted regions of the silicon layer with adjacent non-implanted regions;
forming, through the stencil mask, a capping layer on and substantially in alignment with the implanted regions of the silicon layer;
removing a portion of the non-implanted regions of the silicon layer, wherein the capping layer protects the
implanted regions of the silicon layer during the removing; and
annealing the implanted regions of the silicon layer to form doped polycrystalline silicon emitter regions.

[0003b] According to a second aspect, a method of fabricating alternating N-type and P-type emitter regions of a solar cell is provided, the method comprising:
forming a polycrystalline silicon layer on a thin oxide layer disposed on a monocrystalline silicon substrate;
implanting, through a first stencil mask, dopant impurity atoms of a first conductivity type in the polycrystalline silicon layer to form first implanted regions of the polycrystalline silicon layer adjacent to non-implanted regions;
forming, through the first stencil mask, a first capping layer on and substantially in alignment with the first implanted regions of the polycrystalline silicon layer;
implanting, through a second stencil mask, dopant impurity atoms of a second, opposite, conductivity type in portions of the non-implanted regions of the polycrystalline silicon layer to form second implanted regions of the polycrystalline silicon layer and resulting in remaining non-implanted regions;
forming, through the second stencil mask, a second capping layer on and substantially in alignment with the second implanted regions of the polycrystalline silicon layer;
removing a portion of the remaining non-implanted regions of the polycrystalline silicon layer, wherein the
first and second capping layers protect the first implanted regions and the second implanted regions, respectively, of the polycrystalline silicon layer during the removing; and
annealing the first implanted regions and the second implanted regions of the polycrystalline silicon layer to form doped polycrystalline silicon emitter regions.

[0003c] According to a third aspect, an in-line process apparatus for fabricating an emitter region of a solar cell is provided, the in-line process apparatus comprising: a first station configured to align a stencil mask with a substrate;
a second station configured to implant dopant impurity atoms above the substrate, through the stencil mask; and
a third station configured to form a capping layer above the substrate, through the stencil mask, wherein the stencil mask and the substrate are configured to move together through the second and third stations.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figures 1A-1F illustrate cross-sectional views of various stages in the fabrication of a solar cell, in accordance with an embodiment of the present disclosure.

CLAIMS

What is claimed is:

1. A method of fabricating an emitter region of a solar cell, the method comprising:

forming a silicon layer above a substrate;

implanting, through a stencil mask, dopant impurity atoms in the silicon layer to form implanted regions of the silicon layer with adjacent non-implanted regions;

forming, through the stencil mask, a capping layer on and substantially in alignment with the implanted regions of the silicon layer;

removing a portion of the non-implanted regions of the silicon layer, wherein the capping layer protects the implanted regions of the silicon layer during the removing; and

annealing the implanted regions of the silicon layer to form doped polycrystalline silicon emitter regions.

2. The method of claim 1, wherein the implanting through the stencil mask comprising implanting through a silicon stencil mask, and wherein the silicon stencil mask is positioned on or in close proximity to the silicon layer.

3. The method of claim 1, wherein the implanting and the forming the capping layer are performed in an in-line process apparatus in which the stencil mask and the substrate are moved together through the in-line process apparatus.

4. The method of claim 1, wherein the implanting and the forming the capping layer are performed using a stationary graphite stencil mask.

5. The method of claim 1, wherein forming the capping layer comprises using a deposition technique selected from the group consisting of low pressure chemical vapor deposition

(LPCVD), plasma enhanced chemical vapor deposition (PECVD), high density plasma chemical vapor deposition (HDPCVD) and physical vapor deposition (PVD).

6. The method of claim 1, wherein forming the capping layer comprises depositing at a temperature approximately in the range of 25 – 400 degrees Celsius.

7. The method of claim 1, wherein forming the capping layer comprises forming a material selected from the group consisting of silicon dioxide (SiO_2), silicon nitride (SiN) and silicon oxynitride (SiON).

8. The method of claim 1, further comprising:

removing the capping layer; and

forming conductive contacts on the doped polycrystalline silicon emitter regions.

9. The method of claim 8, wherein removing the non-implanted regions of the silicon layer comprises using a hydroxide-based wet etch process, and wherein removing the capping layer comprises using an HF-based wet etch process.

10. The method of claim 1, further comprising:

forming conductive contacts on the doped polycrystalline silicon emitter regions, the conductive contacts comprising at least a portion of the capping layer.

11. The method of claim 10, wherein forming the capping layer comprises forming a metal selected from the group consisting of titanium (Ti), zirconium (Zr), hafnium (Hf), niobium (Nb), tantalum (Ta), molybdenum (Mo) or tungsten (W), nickel (Ni) and cobalt (Co).

12. A method of fabricating alternating N-type and P-type emitter regions of a solar cell, the method comprising:

forming a polycrystalline silicon layer on a thin oxide layer disposed on a monocrystalline silicon substrate;

implanting, through a first stencil mask, dopant impurity atoms of a first conductivity type in the polycrystalline silicon layer to form first implanted regions of the polycrystalline silicon layer adjacent to non-implanted regions;

forming, through the first stencil mask, a first capping layer on and substantially in alignment with the first implanted regions of the polycrystalline silicon layer;

implanting, through a second stencil mask, dopant impurity atoms of a second, opposite, conductivity type in portions of the non-implanted regions of the polycrystalline silicon layer to form second implanted regions of the polycrystalline silicon layer and resulting in remaining non-implanted regions;

forming, through the second stencil mask, a second capping layer on and substantially in alignment with the second implanted regions of the polycrystalline silicon layer;

removing a portion of the remaining non-implanted regions of the polycrystalline silicon layer, wherein the first and second capping layers protect the first implanted regions and the second implanted regions, respectively, of the polycrystalline silicon layer during the removing; and

annealing the first implanted regions and the second implanted regions of the polycrystalline silicon layer to form doped polycrystalline silicon emitter regions.

13. The method of claim 12, wherein the implanting through the first and second stencil masks comprises implanting through silicon stencil masks, and wherein the first and second silicon stencil masks are sequentially positioned on or in close proximity to the polycrystalline silicon layer.

14. The method of claim 12, wherein the implanting and the forming the first and second capping layers are performed in one or more in-line process apparatuses in which one of the first and second stencil masks and the monocrystalline silicon substrate are moved together through the one or more in-line process apparatuses.

15. The method of claim 12, wherein the implanting and the forming the first capping layer are performed using a first stationary graphite stencil mask, and wherein the implanting and the forming the second capping layer are performed using a second stationary graphite stencil mask.

16. The method of claim 12, wherein removing the remaining non-implanted regions of the polycrystalline silicon layer comprises using a hydroxide-based wet etch process, and wherein the first and second capping layers comprise a material selected from the group consisting of silicon dioxide (SiO_2), silicon nitride (SiN) and silicon oxynitride (SiON), the method further comprising:

removing the first and second capping layers using an HF-based wet etch process; and

forming conductive contacts on the doped polycrystalline silicon emitter regions.

17. The method of claim 12, wherein the capping layer comprises a metal selected from the group consisting of titanium (Ti), zirconium (Zr), hafnium (Hf), niobium (Nb), tantalum (Ta), molybdenum (Mo) or tungsten (W), nickel (Ni) and cobalt (Co), the method further comprising:

forming conductive contacts on the doped polycrystalline silicon emitter regions, the conductive contacts each comprising one of the first or second capping layers.

18. An in-line process apparatus for fabricating an emitter region of a solar cell, the in-line process apparatus comprising:

a first station configured to align a stencil mask with a substrate;

a second station configured to implant dopant impurity atoms above the substrate, through the stencil mask; and

a third station configured to form a capping layer above the substrate, through the stencil mask, wherein the stencil mask and the substrate are configured to move together through the second and third stations.

19. The in-line process apparatus of claim 18, wherein the first station is further configured to align the stencil mask in contact with or in close proximity to the substrate.

20. The in-line process apparatus of claim 18, wherein the second station comprises an ion-implantation or plasma immersion implantation chamber.

21. The in-line process apparatus of claim 18, wherein the third station comprises a deposition chamber selected from the group consisting of a low pressure chemical vapor deposition (LPCVD), a plasma enhanced chemical vapor deposition (PECVD) chamber, a high density plasma chemical vapor deposition (HDPCVD) chamber and a physical vapor deposition (PVD) chamber.