

METHOD OF CONVERTING A SERIES OF M-BIT INFORMATION WORDS INTO A
MODULATED SIGNAL

Method of converting a series of m-bit information words into a modulated signal, method of producing a record carrier, coding device, decoding device, recording device, reading device, signal, as well as a record carrier.

The invention relates to a method of converting a series of m-bit information
5 words to a modulated signal, with m being an integer, in which method an n-bit code word is delivered for each received information word, and the delivered code words alternate with p-bit merging words converted to the modulated signal, and (n+p) exceeding m, and in which the series of information words is converted into a series of alternate code words and merging words according to rules of conversion, so that the corresponding modulated signal satisfies a
10 predetermined criterion. The invention further relates to a method of producing a record carrier on which a signal is recorded obtained according to said method.

The invention further relates to a coding device for performing the method as claimed, this device comprising an m-to-n bit converter for converting the m-bit information words to n-bit code words, and means for selecting the p-bit merging words, and means for
15 converting the alternate n-bit code words and p-bit merging words into a modulated signal.

The invention further relates to a recording device in which a coding device of this type is used.

The invention further relates to a signal.

The invention further relates to a record carrier on which the signal is
20 recorded.

The invention further relates to an apparatus for manufacturing said record carrier, comprising an optical system for scanning a radiation-sensitive layer of a record carrier by a radiation beam and a modulation unit for modulating the radiation beam in such a way that the pattern formed by the radiation beam in the radiation-sensitive layer corresponds
25 to a control signal applied to the modulation unit.

The invention further relates to a decoding device for converting the signal to a series of m-bit information words, this device comprising converting means for converting the signal to a string of bits having a low or high logical value, this bit string containing n-bit

code words which correspond to the information signal portions, and this device comprising converting means for converting the series of code words to the series of information words, while a code word-dependent information word is assigned to each of the code words to be converted.

5 Finally, the invention relates to a reading device in which a decoding device of this type is used.

Such methods, such devices, such a record carrier and such a signal is known
10 from the book "Coding Techniques for Digital Recorders" by K.A. Schouhamer Immink, Chapter 5, Prentice-Hall, 1991, ISBN 0-13-140047-9. In said title, for example, encoders are described, which are used for converting a series of m-bit information words into a series of bits wherein the number of "0"s between two consecutive "1"s lies between d and k. These constraints are also referenced d- and k-constraint, or dk-constraint. In specific prior art
15 methods, (see Pages 114-117 of said title) m-bit information words are converted into n-bit code words in accordance with a conversion table, and where p-bit merging words are inserted between consecutive code words, m, n, p being integers, (n+p) exceeds m, and p exceeds or equals d. The code words and the merging words are chosen such that the dk-constraint of the catenation of alternate code words and merging words is satisfied. The
20 alternate code words and merging words are converted, via a modulo-2 integration operation, into a corresponding signal formed by bit cells having a high or low signal value, a "1"-bit being represented in the modulated signal by a change from the high to the low signal value or vice versa. A "0"-bit is represented by the absence of a change of signal value at a transition between two bit cells. The minimum distance between consecutive transitions of
25 the modulated signal is d+1 bit intervals and the maximum distance between consecutive transitions of the modulated signal is k+1 bit intervals. The dk-constraint is imposed as it is desirable that the system is self-clocking, which requires that consecutive transitions in the modulated signal should not be too far apart, and it is a further requirement that two transitions of the modulated signal should not be following too closely in order to limit inter
30 symbol interference. In addition, the low-frequency components of the modulated signal should be kept as small as possible. Such a signal is also called a dc-free signal. A first reason for using said dc-free signals is that recording channels are not normally responsive to low-frequency components. The suppression of low-frequency components in the signal is also highly advantageous when the signal is read from an optical record carrier on which the

signal is recorded in the track, because then continuous tracking control undisturbed by the recorded signal is possible. A good suppression of the low-frequency components leads to improved tracking with less disturbing audible noise.

An example of the use of such signals to record and read an audio signal on an optical or magneto-optical record carrier can be found in United States Patent Specification 4,501,000. The specification describes the EFM modulation system, which is used for recording information on Compact Discs (CD) or MiniDisc (MD). The EFM-modulated signal is obtained by converting a series of $m(=8)$ -bit information words into a series of $n(=14)$ -bit code words, and where $p(=3)$ merging bits are inserted between consecutive code words. Respective code words of 14 bits satisfy the conditions that at least $d(=2)$ and at most $k(=10)$ "0"s are placed between two consecutive "1"s. In order to satisfy this condition also between code words, 3-bit merging words are used. Four 3-bit merging words of the 8 possible 3-bit merging words are permitted to be used, namely "001", "010", "000", and "100". The remaining possible 3-bit merging words, namely "111", "011", "101", and "110" are not used as they violate the prescribed $d(=2)$ -constraint. One of the four allowed merging words is selected such that the bit string obtained after cascading alternate code words and merging words satisfies the dk -constraint, and that in the corresponding modulo-2 integrated signal the running digital sum value remains substantially constant. The running digital sum value, RDS, at a specific instant is understood to mean the difference between the number of bit cells having the high signal value and the number of bit cells having the low signal value, calculated over the modulated signal portion situated before this specific instant. A substantially constant running digital sum value means that the frequency spectrum of the signal does not comprise frequency components in the low frequency area. By deciding the merging words according to above rules, low-frequency components of the modulated signal can be reduced. The choice for the 3-bit merging words is based on the requirement that, on the one hand the channel signal is substantially dc-free and that also the dk -constraint for the channel signal is satisfied. Decoding of EFM signals is very simple. The 3-bit merging words are skipped by the decoder, and the 14-bit code words are translated, using a look-up table or PLA etc., into the information bytes.

An improved method for suppressing the low-frequency components is described by K.A. Schouhamer Immink and U. Gross in the article entitled "Optimization of Low-frequency Properties of Eight-to-Fourteen Modulation (EFM)", published in the Radio and Electronic Engineer, vol. 53, pp. 63-66, 1983. In said article the authors describe a method, where the selection of a p -bit merging word does not only depend on a single

upcoming code word, but where in contrast the selection is made using q upcoming code words, where q is an integer exceeding 1. From the article cited, it can be concluded that this so-called look-ahead strategy improves the quality of the low-frequency suppression. A significant disadvantage of said strategy is the difficulty of implementing it as the number of operations, such as adding, comparing, buffering, and so on, grows exponentially with the number of code words involved in the selection process. By way of example, a look-ahead strategy using two code words requires $4 \times 4 = 16$ add/compare operations, and a strategy using three code words requires $4 \times 4 \times 4 = 64$ add/compare operations, and so on. For many applications, where speed and power consumption of the selection circuitry is at premium said look-ahead strategy cannot practically be employed.

In a recent article entitled "Weakly constrained codes", published in IEE Electronics Letters, vol. 33, no. 23, pp. 1943-1944, Nov. 1997, the author, K.A. Schouhamer Immink, described a novel type of constrained codes, termed weakly constrained codes. Weakly constrained codes fail to comply with the dk-constraints as they produce sequences that violate the prescribed constraints with (low) probability P . The author argues that if the channel is not free of errors, it is pointless to feed the channel with perfectly constrained sequences. Violation of prescribed dk-constraints offers an additional degree of freedom that can be exploited to reduce the low-frequency components. It is known that violations of the d-constraint, i.e., runs of "0"s smaller than d , are prone to error resulting from inter symbol interference. A violation of the k-constraint could easily result in loss of clock synchronization, which, in turn, could lead to a burst of errors. The method is therefore not very effective as the frequency of violations of the dk-constraint must be small as they will inevitably lead to bit detection errors at the receiver's site.

Information recording has a constant need for increasing the reading and writing speed. The aim of increased reading speed, however, requires higher servo bandwidth of the tracking mechanism, which, in turn, sets more severe restrictions on the suppression of the low-frequency components in the recorded signal. Improved suppression of the low-frequency components is also advantageous for suppressing audible noise arising from the tracking mechanism. For this reason, it is desirable to make as many efforts to prevent the signal from containing low-frequency components.

It is, therefore, an object of the invention to provide a digital modulation method, which is capable of suppressing the low-frequency components with high efficiency, while achieving this goal with a small computational load such as add/compare operations.

A further object of the invention is to provide an information-recording
5 medium such as an optical or magneto-optical disc on which digital data modulated by the invention process is recorded.

A possible solution to the problems inherent in the prior art is based on the observation that prior art methods are overly restrictive in the choice of the merging words as only those merging words are allowed that when alternate merging words and code words are
10 cascaded the prescribed dk-constraint is satisfied.

In a first aspect of the present invention there is provided a digital modulation method for converting m-bit information words into n-bit code words, and where p-bit merging words are inserted between consecutive code words, m, n, p being integers, where (n+p) exceeds m. The code words obey both d- and k-constraint in force, but the merging
15 words are not required to obey said d-constraint. It is known that runs of "0"s smaller than d are prone to error resulting from inter symbol interference. However, as the merging words do not provide information to the receiver, the d-constraint in the merging words can be violated without compromising the reliability of the received code words. Then, as a result of the increase of the size of the set of merging words from which can be selected, the low-
20 frequency components of the modulated signal can significantly be reduced with respect to modulated signals generated under the rules of prior art methods or apparatuses. This embodiment is advantageous in that the presence of low-frequency components in the modulated signal can be significantly better avoided than in the prior art.

A further embodiment of the invention is characterized in that synchronization
25 (sync) words are inserted into the series of code words, the sync words showing bit patterns that cannot occur in the bit stream formed by the catenation of the alternate merging words and code words. The selection circuitry excludes those p-bit merging words that when catenated with the alternate code words would generate the sync pattern. The above excluding rule treats the p-bit merging words that contain u "0"s between consecutive '1's,
30 where u is an integer less than d, as the all "0"s word. This embodiment is advantageous in that in the case the reading mechanism might detect the short "0" runlength as the all "0"s word, false sync patterns are not generated.

These and other objects, features, and advantages of this invention will become more fully apparent from the ensuing description of preferred embodiments of this invention, wherein

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Figure. 1 is a simplified block diagram of an embodiment of the invention;

Figure 2 is a schematic view for use in explanation of modulated data;

Figure 3 is a diagram for use in explanation of the catenation of consecutive code words and the p-bit merging words;

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Figures 4A to 4H are schematic views showing conversion tables for conversion of 8-bit information words into 14-bit code words and vice versa.

In the preferred embodiment of the invention, consecutive n-bit code words are alternated with p-bit merging words. In a first aspect of the invention, the encoder generates a set of allowed p-bit merging words for use between consecutive code words so that the sequence comprised of alternate code words and merging words satisfies the conditions that between the leading "1" in the merging word and the trailing "1" in the code word preceding the merging word, and the trailing "1" in the merging word and the leading "1" in the code word following the merging word are at least d "0"s. In a second aspect of the invention, the encoder selects from said set of allowed merging words that merging word that yields the cumulative dc imbalance nearest zero in the catenation of the code word and that merging word after modulo-2 integration. For example, in the EFM code, where $d=2$, $k=10$, $n=14$, $m=8$, and $p=3$, there are four 3-bit merging words of the 8 possible merging words allowed, namely "001", "010", "000", and "100". In an embodiment of the invention, by way of example, the remaining 3-bit merging words, namely "111", "011", "101", and "110" are allowed to be used. There are, however, three restrictions: firstly, in the cascade of alternate 14-bit code words and 3-bit merging words the $k(=10)$ constraint should not be violated, and secondly in the cascade of alternate 14-bit code words and 3-bit merging words the sync pattern may not be generated, and thirdly, in order to safeguard the reliability of the code words, the number of consecutive "0"s at the beginning or end of the two code words joining the merging word should be at least $d(=2)$. TABLE 1 shows schematically the process of generating the set of allowed merging words, the computation of the corresponding RDS, and the selection of the merging word that yields the least dc-imbalance.

TABLE 1

14-bit word	Merging bits	Next 14-bit word	RDS
01001000100100	000	00100000000100	4
01001000100100	001	00100000000100	10
01001000100100	010	00100000000100	8
01001000100100	011	00100000000100	2
01001000100100	100	00100000000100	6
01001000100100	101	00100000000100	0
01001000100100	110	00100000000100	2
01001000100100	111	00100000000100	8

TABLE 1 shows in detail the translation of the 8-bit information word "01000000", in decimal 64, followed by the translation of the 8-bit information word "01011111", in decimal 95. According to the translation table shown in FIGS. 4A-4H, the information words are translated into the 14-bit code words "01001000100100" and "00100000000100", respectively. For illustrative purposes it is assumed that the RDS at the end of the code word "01001000100100" equals +5. For the specific case in hand all possible 3-bit merging words can be used without violating the prescribed constraints. TABLE 1 shows all possible 3-bit merging words, and it shows the resulting RDS after the merging word and code word have been catenated and integrated modulo-2. According to the invention, the encoder selects that particular merging word resulting in an RDS nearest zero, i.e. it selects "101". The RDS after cascading the merging words "101" and the code word "00100000000100" is thus 0. In this manner the dc level of the modulated signal is maintained at a substantially constant level and the frequency spectrum of the modulated signal will show suppressed low-frequency components. Note that prior art encoders, where the merging bits obey the prescribed (d)-constraint, will select the merging word "000", which will lead to a larger RDS, namely +4. This example shows that signals obtained in accordance with the invented method show a more constant dc level of the modulated signal than those generated by prior art methods.

TABLE 2

14-bit word	Merging bits	Next word	RDS
01001000100100	000	01000001001001	4
01001000100100	001	01000001001001	Not allowed
01001000100100	010	01000001001001	8
01001000100100	011	01000001001001	Not allowed
01001000100100	100	01000001001001	6
01001000100100	101	01000001001001	Not allowed
01001000100100	110	01000001001001	2
01001000100100	111	01000001001001	Not allowed

As a further illustration of the invention, TABLE 2 shows the process of generating all 3-bit merging words in the case code words "01001000100100" and

5 "01000001001001" are catenated. Merging words "001", "011", "101", and "111" are not allowed as the trailing "1" of the merging word and the leading "1" of the code word "01000001001001" are less than $d(=2)$ "0"s apart. If it is assumed that the RDS at the end of the code word "01001000100100" equals +5, then the RDS after a candidate merging word and the 14-bit code word have been catenated and integrated modulo-2 is listed in TABLE 2.

10 According to an aspect of the invention, the encoder selects the merging word resulting in the RDS nearest zero, i.e. it selects "110". The RDS after cascading the merging words "110" and the code word "01000001001001" is thus +2. Note that a prior art encoder, where the merging words obey the prescribed (d)-constraint, will select the merging word "000", which will lead to a larger RDS, namely +4.

15 In the foregoing an explanation was given of an encoder that comprises means for generating all possible p-bit merging words. The encoder further comprises means for selecting that p-bit merging word that satisfies the given constraints and achieves the minimum absolute value of the RDS. It will be obvious for a person skilled in the art that there could be p-bit merging words within the set of possible words that will always lead to

20 the same value of the RDS of the catenation of p-bit merging word and n-bit code word. This property can advantageously be exploited to decrease the selection set, and thus the computational load and/or hardware requirements of the selection circuitry. It can easily be verified that, for example, when $p=3$ the merging words "111" and "010" will always lead to the same value of the RDS. One of the words, for example "111" can be excluded from the

selection set, so that the size of the selection is reduced from 8 to 7 words. It will also be obvious to a person skilled in the art that the p-bit merging bits can be selected on the basis of other criteria than the RDS described in the foregoing.

Preferably, the encoded signal comprises a sequence of q alternate merging words and code words, where q is an integer. Between encoded signal portions are inserted synchronization (sync) signals. Preferably, the sync signal cannot occur in a sequence of the encoded signal. Conventionally, the sync pattern contains a series of s bits having a logical "0", where s is an integer exceeding k, or alternatively the sync pattern consists of two series of k bits having a logical "0" separated by a bit having a logical "1". The p-bit merging word is selected from the candidate merging words such that a catenation of alternate merging words and code words does not contain a pattern equal to the sync pattern. The information is stored in a succession of spaced marks, the lengths of both the marks and the spaces between successive marks being discretely variable in accordance with a succession of code words. It should be appreciated that the merging words "111", "011", "101", and "110" will generate marks or spaces whose length is short with respect to the size of the reading spot. The lengths of the spaces and marks can be so short that the pick up unit cannot observe them. This means that the merging words "111", "011", "101", and "110" will be detected by the decoding device as "000", which in turn means that the detection circuitry could detect false sync patterns or it might lead to a violation of the k constraint. In a preferred embodiment, the merging word selection circuitry can avoid the generation of false sync patterns and/or false k-constraint violation by treating the merging words "111", "011", "101", and "110" as "000" in the computation of the sync pattern or k-constraint. For example, if k=10 then the selection circuitry will exclude merging words that generate sequences such as '00001100000' or '00010100000' and so on as they might lead to false k(=10)-constraint violations. If the sync pattern is '10000000000100000000001' then the selection circuitry will exclude merging words that generate sequences such as '100110000000100000000001' or '100000000000100010100001' and so on that might lead to the generation of a false sync pattern.

An embodiment of the invention is described below referring to the diagrams.

In Fig. 1, reference numeral 1 denotes an input terminal which is supplied with digital data to be recorded on a recording medium such as an optical or magneto-optical disc, numeral 2 refers to a serial-parallel converter for converting input data into data of m parallel bits, and numeral 3 denotes a data converter. The data converter 3 is fed with data bits d1,...,d8 and converts the data bits into 17 channel bits c1,...,c17. The 17-bit word consists

of two parts, namely a 14-bit code word with channel bits $c_1, \dots, c_{14}$, and a 3-bit merging word with channel bits $c_{15}, \dots, c_{17}$. The 14-bit word is generated with a data converter which is made of ROM, PLA, and so on. The data converter translates the data bits $d_1, \dots, d_8$ into output channel bits $c_1, \dots, c_{14}$ in the form of 14 bits. The code conversion tables shown in

5 Figs. 4A to 4H comply with the rule that the $n(=14)$ code bits (c_1 to c_{14}) obtained by such modulator never fails to place at least $k(=2)$ and at most $d(=10)$ "0"s between consecutive "1"s. Clock generator 6 generates a clocking signal for the circuitry. The data converter 3 has additional means to generate the 3-bit word, $c_{15}, \dots, c_{17}$. The additional means can either consist of ROM, PLA and so on or it can be built using a computer that has been

10 programmed to determine the 3-bit word such that particular specifications described above are satisfied.

Fig. 2 shows an embodiment for a coding device according to the invention by which the method described above can be carried out. In Fig. 2 reference numeral 21 refers to an input terminal supplied with the signal data to be translated prior to be recorded on a

15 recording medium, numeral 22 refers to a serial-to-parallel converter for converting input data into data of 8 parallel bits, and numeral 23 denotes a data converter. The data converter 23, which consists of ROM, PLA and others, is supplied with data bits $d_1, \dots, d_8$ in the form of 8 bits, and supplies the code word $c_1, c_2, \dots, c_{14}$ in the form of 14 bits. Conversion tables can be found in Figs 4A to 4H, which are the same as the formerly proposed EFM

20 modulation. The 14-bit data is converted from a parallel into a serial converter using converter 24. The coupling bit adder, 25, generates the various candidate merging words that satisfy the prescribed d_k -constraint. The set of candidate merging words is preferably stored in ROM, PLA and others. The selection circuit, 26, selects from the candidates the one with the RDS nearest zero. The selection circuit comprises an arithmetic unit for computing the

25 RDS of each possible candidate merging word catenated by the 14-bit code word. The signal generator 29 generates signals for timing control for the selection circuitry 27. The modulated signal obtained after modulo-2 integration of the catenation of alternate merging words and code words, taken out from terminals 29 and 30, is forwarded to an optical pickup or other recording means via a recording amplifier and recorded onto an optical carrier, not shown,

30 such as optical or magneto-optical disc or tape or other recording medium.

Fig.3 shows the catenation of two $m(=14)$ -bit code words and the p -bit merging words. In the preferred embodiment the value of p is 3 or 2.

Fig. 4A-H shows the preferred conversion tables for translating the 8-bit data words, $d_1, \dots, d_8$, into the 14-bit code word $c_1, \dots, c_{14}$. The conversion tables comply with the

rule that there are always at least two and at most ten "0"s between consecutive "1"s. It will be understood that code conversion tables different from those shown in Fig. 4A-H can be used.

It will be appreciated from the foregoing description that the present invention provides an improved system for recording and playing back digital information on a disc-shaped record. The information is stored in a succession of spaced marks, the lengths of both the marks and the spaces between successive marks being discretely variable in accordance with a succession of code words. The digital information is thereby stored with an improved suppression of the low-frequency components of the recording signal.

Although the present invention has been described in detail with reference to its presently preferred embodiment, it will be understood by those of ordinary skill in the art that various modifications can be made without departing from the spirit and scope of the invention. Accordingly, it is not intended that the invention be limited, except as by the appended claims. Any reference signs do not limit the scope of the claims. The word "comprising" does not exclude the presence of other elements or steps than those listed in a claim. Use of the word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements.

CLAIMS:

1. A method of coding a sequence of binary data bits into a sequence of binary channel bits, wherein consecutive and sequential blocks of m data bits, where m an integer, are coded into sequential n -bit code words, where n an integer exceeding m , in accordance with a translation table, wherein the code words satisfy a dk -constraint such that consecutive
5 "1"s are separated by at least d and at most k "0"s, and where between said consecutive code words a p -bit merging word, where p an integer, is inserted, the catenation of said alternate code words and merging words satisfying the conditions that between the leading "1" in the merging word and the trailing "1" in the code word preceding the merging word are at least d "0"s, and that between the trailing "1" in the merging word and the leading "1" in the code
10 word following the merging word are at least d "0"s, characterized in that the merging words are not required to obey said d constraint.
2. A method as claimed in Claim 1, wherein p -bit merging words are operative for constraining the number of "0"s between consecutive "1"s of the catenation of the
15 alternate code words and merging words to at maximum s , where s an integer equal to or exceeding k .
3. A method as claimed in Claim 1 and 2, wherein p -bit merging words are operative for diminishing the cumulative dc imbalance of the signal generated after modulo-2
20 integration of the catenation of the alternate code words and merging words.
4. A method of encoding a binary digital signal according to Claims 1, 2, and 3, wherein $d=2$, $k=10$, $m=8$, $n=14$, and $p=3$.
- 25 5. A method of encoding a binary digital signal according to Claims 1, 2 and 3, wherein $d=2$, $k=10$, $m=8$, $n=14$, and $p=2$.
6. A decoder for decoding an encoded signal in accordance with method claimed in any of the preceding Claims 1 to 5.

7. An information recording medium having recorded thereon an information structure formed in response to the method of coding as claimed in any of the Claims 1 to 5, inclusive.

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8. An information recording medium according to Claim 7, wherein said information medium comprises an optically readable record carrier.

9. A coding device for carrying out the method of coding a sequence of binary data bits into a sequence of binary channel bits as claimed in any of the Claims 1 to 5, inclusive.

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