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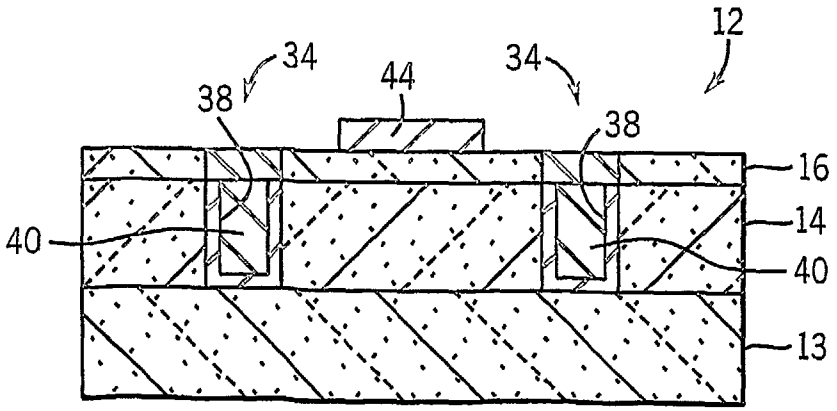
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(54) Title: SHALLOW TRENCH ISOLATION PROCESS FOR STRAINED SILICON PROCESSES



(57) Abstract: A method of manufacturing an integrated circuit (IC) utilizes a shallow trench isolation (STI) technique. The shallow trench isolation technique is used in strained silicon (SMOS) process. The liner for the trench is formed from a layer deposited in a low temperature process which reduces germanium outgassing. The low temperature process can be an LPCVD. An annealing step can further be performed on the liner.

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