

Abstract

Pulsed Signal Generator

5 A pulse width modulated (PWM) voltage generator includes a
phase locked loop (PLL) for generating a clock square-wave signal at
a frequency which is twice that of a desired resolution frequency of
the PWM output signal. A PWM controller (14) receives the clock
square-wave signal and a data signal and provides a PWM output
10 having a duty cycle determined by the data signal at the frequency
of the clock square-wave signal. A switching circuit coupled to the
PWM controller (14) receives a signal from a frequency divider (16),
which forms part of the PLL, and switches an output of the
generator to be floating for the first half of the PWM frame cycle so
15 that the PWM output signal does not include the PWM output from
the PWM controller when the clock square-wave signal has non-
uniform frequency. But, because of the doubled frequency of the
clock square-wave signal, the average frequency of the PWM output
signal is still at the desired resolution frequency and the duty cycle
20 of the PWM output signal is as determined by the data signal.

FIG. 1