PROCESS FOR FORMING AND CONTROLLING ROUGH INTERFACES

DESCRIPTION

TECHNICAL FIELD AND PRIOR ART

The invention relates to the field of microstructure manufacturing as well as treating substrates in semiconductor materials.

In microelectronics, certain operations, such as bonding operations, require that the surfaces to be bonded are as smooth as possible. But the manufacturing of certain devices, particularly the type implementing a membrane or mobile part, may necessitate having recourse to surfaces that face each other but that cannot adhere to each other, in order to be able to justly prevent untimely bonding of the membrane on the facing surface and to be able to maintain mobility of this membrane.

Therefore document FR 2 857 953 discloses a process of manufacturing BSOI type structures in which a so-called structured zone is made, preventing bonding to another surface. This type of structure is interesting in the MEMS fabrication, and more particularly in the case where the superficial silicon membrane must be released to manufacture sensors.

During the release step, a step which comprises for example an underlying oxide attack, or during operation of the sensor, the membrane bonds to the substrate, thereby inducing dysfunction of the component.

As explained in the document above, a BSOI substrate that comprises a rough buried interface avoids this problem; the roughness of the buried interface prevents any bonding between the membrane and the support.

In document FR 2 857 953, roughening of the surface is done by various techniques, for example by the use of "unibond ® negatives", produced by the "Smart Cut ™" process. Such a process is described in FR 2 681 472 or alternately in B. Aspar et al., "The generic nature of the smart cut process for thin film transfer," J. of Elec. Material, vol. 30, No. 7, 2001.

To obtain the buried roughness adapted to different antisticking BSOI substrates, it is therefore necessary to supply negatives having this particular roughness.

Therefore the problem of finding a new process allowing such substrates or negatives having a particular surface roughness to be made is posed, a roughness that particularly allows, during manufacture of membranes or mobile parts of integrated sensors, the bonding effects mentioned above to be avoided.

DISCLOSURE OF THE INVENTION

The invention proposed furthermore allows greater flexibility regarding the supply or manufacture of substrates with specific roughness, since it allows the roughness of the substrates to be adapted according to need.

A process according to the invention allows "Unibond®" wafers (also called "negatives") to be recycled by adapting their surface roughness to the application of desired MEMS, for example in the context of antisticking BSOI manufacturing.

The invention first relates to a process for making a rough interface with a predetermined roughness R2 in a semiconductor substrate comprising:

- the selection of a semiconductor substrate, presenting a surface roughness of R1>R2,
- a thermal oxidation step for this substrate until an oxide - semiconductor interface with a roughness of R2 is obtained.

Thermal oxidation is preferably carried out on a thickness that is greater than or equal to 0.2 µm or 0.5 µm, and for example under dry or wet atmosphere.

The semiconductor substrate selected comprises for example a HF (high frequency) roughness between 5 and 10 nm RMS and/or a LF (low frequency) roughness between 2 and 10 nm RMS.

The semiconductor substrate with roughness R1 may be a negative issued from the manufacture of SOI structures by the Smart Cut ™ technology (substrate fracture technique).

The invention also relates to a process of forming a semiconductor component with a rough buried interface comprising:

- the formation of a rough oxide/silicon interface with a predetermined roughness R2 in a first semiconductor substrate according to a process according to the invention, such as explained above,
- preparation of the oxidized surface in view of an assembly with a second substrate,
- assembly of the oxide surface and the second substrate.

The second substrate may be a bulk substrate, or even be obtained by a process according to the invention, such as explained above.

One of the two substrates may then be thinned, for example by a mechanical technique and/or chemical technique and/or fracture of the substrate.

This final structure may then be used for example for making antisticking structures, which are BSOI structures having a rough buried interface. During production of the components on the final structure, and particularly mobile parts and membranes, at least one portion of the oxide or oxidized material may be eliminated, for example by etching through at least one opening made in one of the two substrates, typically in the superficial layer of an SOI substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

- Figures 1A and 1B represent obtaining a "Unibond" type negative or rough substrate.
- Figures 2A-2C represent an embodiment of the invention.
- Figure 3 represents the evolution of haze according to the thickness of oxide formed.
- Figures 4A and 4B represent the assembly of a substrate according to the invention with another substrate.
- Figures 5A and 5B represent the assembly of two substrates according to the invention.
- Figure 6 represents a component obtained according to the invention, with a cavity buried under a membrane.

DETAILED DISCLOSURE OF PARTICULAR EMBODIMENTS

First we will explain how a rough substrate may be obtained. In the example chosen, it will be a "Unibond®" wafer cited as a negative, obtained from a Smart Cut™ process or substrate fracture.

As illustrated in Figure 1A, a first semiconductor substrate 6 is selected. This substrate 6 may be for example in "bulk" silicon.

On this substrate an insulating zone or layer 4 is made by thermal oxidation for example (silicon oxide SiO_2 will be taken as an example) having a typical thickness on the order of several hundreds of nm, for example between 100 nm and 500 nm.

Atomic or ionic implantation is performed in this semiconductor substrate 6, forming a thin layer 8 that extends substantially parallel to a surface 11 of the substrate 6. In fact, a layer or plane of embrittlement or fracture is formed delimiting in the volume of the substrate 6 a lower region 10 intended to comprise a thin film and an upper region 13 comprising the substrate 6 mass. This implantation is generally hydrogen implantation, but may also be done by using other species or even H/He co-implantation.

This substrate 6 thus prepared is then assembled by a molecular bonding technique with a second substrate 2, for example in silicon. Concerning these bonding techniques, one may refer to the work of Q.Y. Tong and U. Goesele, "Semi-conductor Wafer Bonding," (Science and Technology), Wiley Interscience Publications.

A part of substrate 6 is then detached by treatment allowing a fracture to be made along the embrittlement plane 8. An example of this technique is described in the article by A. J. Auberton-Hervé et al., "Why can Smart-Cut change the future of microelectronics?" published in the International Journal of High Speed Electronics and Systems, Vol. 10, No. 1 (2000), pp. 131-146.

On the one hand a semiconductor component or element 12, and on the other hand a residual part 16 of substrate 6 are formed, presenting a rough surface 14, due to the fracture. This residual part comprises a rough starting substrate for the rest of the explanations below.

According to an embodiment of the invention, illustrated in Figures 2A-2C, a rough substrate 16 or "Unibond®" negative, resulting for example from a process such as explained above, is selected. This is then the peeled part of the substrate after layer transfer by the "Smart Cut™" technique.

For example, it is in silicon.

Surface 14 of this substrate 16 presents a certain roughness R1 (Figure 2A). The roughness varies for example from 5 nm to 10 nm RMS (measured by atomic force microscopy (AFM) on 5*5 μm^2) in the high frequency domain and from 2 nm to 10 nm RMS (measured by a mechanical surface roughness measuring instrument with a 2 µm point of 500 µm scans) in the low frequency domain.

According to the invention, the roughness of the selected substrate 16 adapted, for example according to the MEMS type (application type, sensor type, membrane dimensions and characteristics, etc.).

For this purpose, desoxidation of the negative substrate 16 is preferentially performed. The latter is then cleaned by CARO RCA or ozone RCA type cleaning. A possible cleaning with TMAH (tetramethylammonium hydroxide chemical etching step) allows approximately 2 to 3 µm to be thinned to eliminate an area disturbed by the implantation step. Then the substrate 16 is oxidized under dry or wet atmosphere for a thickness of, for example, between 0.2 µm and 2 µm, preferentially on the order of 0.5 µm.

Considering the roughness of surface 14 of substrate 16, the oxidation front 22 is irregular and therefore will transfer part of the roughness to an oxide/silicon interface that will be in substrate 16 at a depth that will depend on the oxidation conditions, and particularly on the temperature and duration during which it is performed. Figures 2B and 2C represent the same substrate 16, respectively after oxidation of duration t1 and after oxidation of duration t2 > t1, these oxidations having been performed at the same temperature. The oxide layer 20 of the first case has a thickness e1 inferior to e2, the thickness of the oxide layer 20' of the second case, while the respective roughnesses are:

$R'2<R2<R1$.

By controlling the thickness e of the oxide generated, the spatial frequencies and amplitude (RMS, PV) of the desired final roughness (R2) at the level of the oxide/silicon interface are controlled.

According to the oxide 20, '20' thickness generated, the roughness is therefore more or less reduced, which allows the resulting roughness at the level of the oxide/silicon interface (R2) to be controlled.

Figure 3 represents the evolution of the "haze" measured on the silicon surface (after oxide removal) with TENCOR (6200) surfscan type equipment according to the thickness e of oxide obtained after the oxidation step. The "haze" is connected to the light diffused by the surface and is therefore representative of the roughness of this surface. The "haze" therefore allows information on the surface roughness to be obtained according to the thickness of oxide formed. One can see that, in the 0.5 µm - 2 µm or 1 µm - 2 µm range of thicknesses, and even beyond 2 µm,

roughness is highly reduced while at the same time oxide thickness is increased. But an effect may also be obtained for thicknesses greater than 0.2 μm.

The initial rough substrate 16 may therefore be treated in view of its utilization for the fabrication of different categories of components.

Such a substrate treated according to the invention, comprising a predetermined rough buried oxide/silicon interface may be utilized for different applications.

A substrate treated according to the invention may therefore be employed for manufacturing antisticking BSOI substrates, as "top" and/or support substrates.

Bonding of the oxidized substrate to the rough interface may be carried out. Preparing the surface of the oxide is then recommended; an optional mechanical peripheral edge removal step may also be done in order to eliminate the crown that was not eliminated by oxidation.

As illustrated in Figure 4A, a mechanical polishing step may be performed to restore good surface roughness (that is, a roughness adapted this time to bonding) of the oxide layer 20 (or 20').

As illustrated in Figure 4B, bonding, for example direct or molecular adhesion bonding, may then be performed on a second substrate 34, for example in bulk silicon. This second substrate 34 may then be thinned. Any thinning technique, for example, a mechanical technique, a chemical technique, a mechanical chemical technique or the "Smart Cut ™" process may be implemented.

Direct bonding may also be carried out on a second substrate 44, itself having a rough buried interface 42

(Figure 5A). This substrate was preferably obtained according to the process described above.

Then, the assembled structure may be submitted to thermal treatment to reinforce the bonding interface and one or more thinning steps until a BSOI 46 structure is obtained comprising one or two rough oxide/silicon interfaces. Figure 5B represents such a structure with two rough interfaces 22, 42 and one residual layer 45 of the second substrate.

During production of integrated sensor membranes or mobile parts, part of oxide 20 may then be locally removed by etching through openings 111, 113 made in the residual layer 45. One may therefore locally create cavities under membranes. The rough interface 42 prevents untimely bonding or adherence of the membrane on the substrate 14.

Therefore Figure 6 represents such a cavity 50 in substrate 46 after etching of the oxide layer 20 through openings 111, 113 of layer 45, whose portion situated above the cavity 50 forms a membrane.

The examples given above implement a silicon substrate. But the invention may be applied to all semiconductor substrates that may be oxidized, and particularly: monocrystalline Si, polycrystalline Si, amorphous Si, SiC.

CLAIMS

1. A process for forming a semiconductor component with a rough buried interface from an initial substrate (6), comprising:

   a) the formation of a rough interface (22, 22') with a predetermined , roughness R2, in a first semiconductor substrate (16), with:
      * the selection of a semiconductor substrate (16) being obtained by fracture of the initial substrate (6) presenting a surface (14) of roughness R1>R2,
      * a thermal oxidation step for this substrate being carried out on a thickness greater than or equal to 0.2 µm, until an oxide-semiconductor (22, 22') interface with roughness R2 is obtained,
   b) preparation of the oxidized surface of this first semiconductor substrate, in view of assembly with a second substrate (34, 44),
   c) the assembly of the surface of the oxide of the first substrate and of the second substrate (34, 44).

2. The process according to claim 1, the thermal oxidation being done under dry or wet atmosphere.

3. The process according to claim 1 or 2, the semiconductor substrate selected comprising an HF roughness between 5 and 10 nm RMS.

4. The process according to one of claims 1 to 3, the semiconductor substrate selected comprising an LF roughness between 2 and 10 nm RMS.

5. The process according to one of claims 1 to 4, the second substrate being a raw or bulk semiconductor substrate (34).

6. The process according to one of claims 1 to 5, the second substrate (44) itself being obtained by a process according to one of claims 1 to 5.

7. The process according to one of claims 1 to 6, one of the two substrates then being thinned, for example by a mechanical and/or chemical technique, and/or substrate fracture.

8. The process according to one of claims 1 to 7, at least one portion of the oxide formed in the first or in the second semiconductor substrate being eliminated.

9. The process according to claim 8, the elimination of a portion of the oxide being carried out by etching through at least one opening (111, 113) made in one of the two substrates.