

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor device and a method of manufacturing the same and more particularly to a semiconductor device in which a lead frame of a multilayered structure is bonded on an electrode of a semiconductor chip and a manufacturing method thereof.

Description of the Related Art

As a constitution for connecting a semiconductor integrated circuit device (hereinafter referred to as a semiconductor chip) to an external circuit, a lead frame has been used generally so far. Namely, a semiconductor chip is bonded and secured to a lead frame, and an electrode pad (bonding pad) disposed on a semiconductor chip is electrically connected with designated lead pins on the lead frame, and the leads are connected to an interconnecting land of a printed circuit substrate as an external circuit in a state of protruding lead pins along the circumference of the semiconductor chip.

In this case, surface mounting (SMT) is conducted particularly in a case of requiring highly dense mounting. As an example of the surface mounting using a lead frame, it

is generally adopted a constitution in which a gull wing type lead is formed with the top end of the lead pin is bent, for example, in a L-shaped configuration, and a flat portion at the top end of the L-shaped configuration is electrically connected with the interconnecting land of the printed circuit substrate.

On the other hand, as a method of electrically connecting an electrode pad on the semiconductor chip and the designated lead of the lead frame, it was formerly adopted a wire bonding method of hot press bonding fine gold wires or fine aluminum wires while using ultrasonic waves together, whereas wireless bonding has been generally applied in recent years instead of such wire bonding.

As a wireless bonding method, there is a face-down bonding of bonding an electrode pad on a semiconductor chip and one end of a lead pin in direct or indirect contact with the semiconductor chip being faced down.

On the other hand, along with progress of more highly dense mounting, the pitch between the electrode pads has been narrowed and a fine wire lead is required to be connected with the electrode pad, so that as a constitution of a lead frame applied to the highly dense face-down bonding as described above, a fine wire lead with a multilayered structure formed by applying gold plating on a fine wire

manufactured from a copper foil as a base has also been known.

Furthermore, it has also been known a constitution of forming a thin gold layer of about 30 μm thickness by vapor deposition with an aim of improving the connection property to a gold plated portion to be connected with an electrode pad of a fine wire lead of a multilayered structure in which gold plating is applied on the copper foil.

However, in the fine wire lead applied with gold plating on the copper foil as described above, since a copper foil is bonded to a polyimide tape by an adhesive, then a fine wire lead is formed by selectively etching to eliminate the copper foil and successively plating the surface with gold as a manufacturing step of the fine wire lead, the cross sectional area of the fine wire lead is liable to be reduced to less than a predetermined size by the occurrence of side etching, so that the strength of the fine wire lead is weakened remarkably to result in a problem that the fine wire lead tends to undergo deformation such as bending upon forming the gold layer by gold plating.

Further, in a method of forming a thin gold layer further on gold plating of the fine wire lead of the multilayered structure, since the thin gold layer is formed by a vapor deposition method, it takes a long time for vapor deposition to result in a problem in view of manufacturing

efficiency. Further, it is difficult by this method to attain the film thickness of the thin gold layer of 3 μm or more and, further, the accuracy of the film thickness is low to result in a problem that the quality control is difficult.

In addition, when the lead frame of the multilayered structure is intended to be bonded with the electrode pad of the semiconductor chip, a portion below the electrode pad of the semiconductor chip suffers from injury by pressure or ultrasonic vibrations applied during bonding, and cracking is induced in an interlayer film between the electrode pad and silicon substrate, to bring about disadvantage that electric leakage is caused between the electrode pad and silicon or the silicon substrate is partially cracked to bring about peeling of the bonded portion.

SUMMARY OF THE INVENTION

The present invention has been accomplished in order to solve the foregoing problem in the related art and has an object of providing a semiconductor device for attaining bonding at high reliability by moderating thermal and mechanical impact shocks during bonding between an electrode pad and a fine wire lead frame of a multilayered structure, and a manufacturing method thereof.

A method of manufacturing a semiconductor device

according to the present invention for solving the foregoing subject comprises the steps of forming a metal bump of a first kind of metal on an electrode pad of a semiconductor chip; and bonding the electrode pad and a lead frame of a multilayered structure partially metal plated with a second kind of metal by way of the metal bump at least by heating and pressurization.

In accordance with the constitution described above, since the metal bump absorbs vibrations, injuries of the semiconductor chip liable to occur in a portion below the electrode pad is suppressed.

Further, a method of manufacturing a semiconductor device according to the present invention has a feature of conducting bonding by applying heating, pressurization and ultrasonic waves.

In accordance with the constitution described above, since ultrasonic energy is applied in addition to the application of heat and pressure upon bonding, an object to be bonded is caused to vibrate and efficient bonding is attained by the vibrations.

Alternately, when a method of manufacturing a semiconductor device according to the present invention comprises a step of treating at least the surface of the bonding portion of the lead frame with plasma irradiation

prior to bonding of the lead frame to the metal bump, contaminants deposited on the surface are eliminated by which the cause bringing about troubles upon bonding can be eliminated.

A semiconductor device according to the present invention has a feature wherein a metal bump with a first kind of metal is formed on an electrode pad of a semiconductor chip, and a lead frame of a multilayered structure having a second kind of metal disposed on the surface thereof is bonded with the metal bump.

In accordance with the constitution described above, thermal or mechanical impacts transmitted by way of the lead frame from the outside of the semiconductor device are absorbed or attenuated in the metal bump and, as a result, undesired effects by the impacts on the electrode pad or the semiconductor chip can be moderated.

Alternatively, when the semiconductor device according to the present invention is constituted such that the first kind of metal and second kind of metal are constituted with an identical metal, bonding between them to each other at good quality can be attained upon melting due to excellent compatibility provided in the bonding portion between the metal bump and the lead frame.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic cross sectional view of a first embodiment of a semiconductor device according to the present invention.

Fig. 2 is a cross sectional view of a step in a manufacturing method for an example of a lead frame applied to the present invention.

Fig. 3 is an explanatory view for a step succeeding to Fig. 2.

Fig. 4 is an explanatory view for a step succeeding to Fig. 3.

Fig. 5 is an explanatory view for a step succeeding to Fig. 4.

Fig. 6 is an explanatory view for a step succeeding to Fig. 5.

Fig. 7 is an explanatory view for a step succeeding to Fig. 6.

Fig. 8 is an explanatory view for a step succeeding to Fig. 7.

Fig. 9 is a schematic cross sectional view for a second embodiment of a semiconductor device according to the present invention.

Fig. 10 is a schematic cross sectional view for a third embodiment of a semiconductor device according to the

present invention.

Fig. 11 is a schematic cross sectional view for a fourth embodiment of a semiconductor device according to the present invention.

Fig. 12 is a schematic cross sectional view for a fifth embodiment of a semiconductor device according to the present invention.

Fig. 13 is a schematic cross sectional view for sixth embodiment of a semiconductor device according to the present invention.

Fig. 14 is a schematic cross sectional view for a seventh embodiment of a semiconductor device according to the present invention.

Fig. 15 is a schematic cross sectional view for a eighth embodiment of a semiconductor device according to the present invention.

Fig. 16 is a schematic cross sectional view for a ninth embodiment of a semiconductor device according to the present invention.

Fig. 17 is a schematic cross sectional view for a tenth embodiment of a semiconductor device according to the present invention.

Fig. 18 is an explanatory view for a step of a first embodiment for a manufacturing method of a semiconductor

device according to the present invention.

Fig. 19 is an explanatory view for a step succeeding to Fig. 18.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now, preferred embodiments of the present invention are to be explained specifically with reference to the accompanying drawings. The embodiments to be described are a portion of preferred embodiments of the present invention which are variously defined preferably in view of technical constitution, but the scope of the present invention is not restricted to the embodiments unless it is otherwise specified in the subsequent explanation that the invention is limited.

Fig. 1 is a schematic cross sectional view of a first embodiment of a semiconductor device according to the present invention.

As shown in Fig. 1, in a semiconductor device 1 according to the present invention, a metal bump 5 made of a first kind of metal M1 is formed on an electrode pad 3 of a semiconductor chip 2, and a fine wire lead 7 of a three-layered constitution of a lead frame 6 is bonded to the metal bump 5.

The fine wire lead 7 comprises a lower layer 7a

constituted with a second kind of metal M2, an intermediate layer 7b and an upper layer 7c.

In this case, the first kind of metal M1 and the second kind of metal M2 may be constituted with an identical metal.

Further, since the layer structure of a multilayered lead frame used as a part in a semiconductor device and a manufacturing method thereof according to the present invention is characteristic, particularly, to the manufacturing method, outline thereof is to be explained below.

The multilayered lead frame comprises a layer that is abutted against and bonded with the metal bump as a lower layer, a layer constituting an upper surface as an upper layer and a layer situated between the upper layer and the lower layer as an intermediate layer. The constitution with no intermediate layer comprises a two-layered structure as a whole, a constitution with one layer of the intermediate layer comprises a three-layered structure as a whole and a constitution with two intermediate layers comprises a 4-layered structure as a whole. The lower layer is constituted with the second kind of metal.

Gold, silver, palladium or the like is preferred as the second kind of metal constituting the lower layer.

Accordingly, preferred examples of the multilayered lead frame used in the present invention include the following three-layered structures as example.

- (1) A three-layered structure comprising a lower layer of gold, an intermediate layer of nickel and an upper layer of copper.
- (2) A three-layered structure comprising a lower layer of gold, an intermediate layer of palladium and an upper layer of copper.
- (3) A three-layered structure comprising a lower layer of silver, an intermediate layer of palladium and an upper layer of copper.
- (4) A three-layered structure comprising a lower layer of silver, an intermediate layer of nickel and an upper layer of copper.
- (5) A three-layered structure comprising a lower layer of palladium, an intermediate layer of nickel and an upper layer of copper.

Further, examples of the two-layered structure include the followings.

- (6) A two-layered structure comprising a lower layer of gold and an upper layer of copper.
- (7) A two-layered structure comprising a lower layer of silver and an upper layer of copper.

(8) A two-layered structure comprising a lower layer of palladium and an upper layer of copper.

A metal layer identical with the intermediate layer, the lower layer or only the lower layer may be disposed on copper due to the reason in view of the process.

Among them described above, a method of manufacturing a lead frame for the case (6) comprising the lower layer of metal and the upper layer of copper, in which metal is further formed on the upper layer of copper in view of process is to be explained with reference to Fig. 2 to Fig. 8.

Fig. 2 to Fig. 8 represent cross sectional views on each step in the method of manufacturing the lead frame.

As shown in Fig. 2, a copper plate 11 is prepared as a substrate, and a pattern layer 12 as shown in Fig. 3 is selectively formed on the copper plate 11. After forming the pattern layer 12, gold is plated on the surface of the copper plate 11 on the side formed with the pattern layer 12 using the pattern layer 12 as a mask, to form a lower gold layer 23a, for example, of $0.1\ \mu\text{m}$ to $5\ \mu\text{m}$ thickness. Copper is plated on the lower gold layer 23a, to form a copper layer 23b, for example, of $5\ \mu\text{m}$ to $20\ \mu\text{m}$ thickness as shown in Fig. 5.

After forming the copper layer 23b, gold is plated on the copper layer 23b in the same manner as in the case of

forming the lower gold layer 23a, to form an upper gold layer 23c, for example, of $0.1\ \mu\text{m}$ to $5\ \mu\text{m}$ thickness as shown in Fig. 6, thereby forming a fine wire lead 23 comprising a three-layered structure of the lower gold layer 23a, the copper layer 23b and the upper gold layer 23c.

After forming the upper gold layer 23c, the pattern layer 12 is removed, and an insulation resist film 14 is formed selectively excepting for the top end of the fine wire lead 23 as shown in Fig. 7. Subsequently, the copper layer 11 is etched selectively. An etching stop layer in this case is a lower gold layer 23a.

Thus, as shown in Fig. 8, a lead frame having a fine wire lead 23 of the three layered structure having the lower gold layer 3a on one surface and the upper gold layer 23c on the other surface with the copper layer 13b being inserted between the upper gold layer 23a and the lower gold layer 23c.

Fig. 9 is a schematic cross sectional view of a second embodiment of a semiconductor device according to the present invention.

As shown in the figure, in a semiconductor device 201 according to the present invention, a metal bump 205 made of gold (Au), silver (Ag), palladium (Pd), aluminum (Al) or copper (Cu) as the first kind of metal is formed on an electrode pad 203 of a semiconductor chip 202, and a lead

frame 207 having a fine wire lead 206 of a three-layered structure in which a gold (Au) layer as the second kind of metal is disposed as a lower layer 206a at the lower end face is bonded with the metal bump 205.

An intermediate layer 206b of the fine wire lead 206 is made of copper (Cu) and an upper layer 206c thereof is made of gold (Au).

Fig. 10 is a schematic cross sectional view of a third embodiment of a semiconductor device according to the present invention.

As shown in the figure, in a semiconductor device 301 according to the present invention, a metal bump 305 made of gold (Au), silver (Ag), palladium (Pd), aluminum (Al) or copper (Cu) as the first kind of metal is formed on an electrode pad 303 of a semiconductor chip 302, and a lead frame 307 having a fine wire lead 306 of a three-layered structure in which a gold (Au) layer as the second kind of metal is disposed as a lower layer 306a at the lower end face is bonded with the metal bump 305.

An intermediate layer 306b of the fine wire lead 306 is made of nickel (Ni) and an upper layer 306c thereof is made of copper (Cu).

Fig. 11 is a schematic cross sectional view of a fourth embodiment of a semiconductor device according to the

present invention.

As shown in the figure, in a semiconductor device 401 according to the present invention, a metal bump 405 made of gold (Au), silver (Ag), palladium (Pd), aluminum (Al) or copper (Cu) as the first kind of metal is formed on an electrode pad 403 of a semiconductor chip 402, and a lead frame 407 having a fine wire lead 406 of a three-layered structure in which a gold (Au) layer as the second kind of metal is disposed as a lower layer 406a at the lower end face is bonded with the metal bump 405.

An intermediate layer 406b of the fine wire lead 406 is made of palladium (Pd) and an upper layer 406c thereof is made of copper (Cu).

Fig. 12 is a schematic cross sectional view of a fifth embodiment of a semiconductor device according to the present invention.

As shown in the figure, in a semiconductor device 501 according to the present invention, a metal bump 505 made of gold (Au), silver (Ag), palladium (Pd), aluminum (Al) or copper (Cu) as the first kind of metal is formed on an electrode pad 503 of a semiconductor chip 502, and a lead frame 507 having a fine wire lead 506 of a three-layered structure in which a gold (Au) layer as the second kind of metal is disposed as a lower layer 506a at the lower end face

is bonded with the metal bump 505.

An intermediate layer 506b of the fine wire lead 506 is made of palladium (Pd) and an upper layer 506c thereof is made of copper (Cu).

Fig. 13 is a schematic cross sectional view of a sixth embodiment of a semiconductor device according to the present invention.

As shown in the figure, in a semiconductor device 601 according to the present invention, a metal bump 605 made of gold (Au), silver (Ag), palladium (Pd), aluminum (Al) or copper (Cu) as the first kind of metal is formed on an electrode pad 603 of a semiconductor chip 602, and a lead frame 607 having a fine wire lead 606 of a three-layered structure in which a gold (Au) layer as the second kind of metal is disposed as a lower layer 606a at the lower end face is bonded with the metal bump 605.

An intermediate layer 606b of the fine wire lead 606 is made of nickel (Ni) and an upper layer 606c thereof is made of copper (Cu).

Fig. 14 is a schematic cross sectional view of a seventh embodiment of a semiconductor device according to the present invention.

As shown in the figure, in a semiconductor device 701 according to the present invention, a metal bump 705 made of

gold (Au), silver (Ag), palladium (Pd), aluminum (Al) or copper (Cu) as the first kind of metal is formed on an electrode pad 703 of a semiconductor chip 702, and a lead frame 707 having a fine wire lead 706 of a three-layered structure in which a gold (Au) layer as the second kind of metal is disposed as a lower layer 706a at the lower end face is bonded with the metal bump 705.

An intermediate layer 706b of the fine wire lead 706 is made of nickel (Ni) and an upper layer 706c thereof is made of copper (Cu).

Fig. 15 is a schematic cross sectional view of a eighth embodiment of a semiconductor device according to the present invention.

As shown in the figure, in a semiconductor device 801 according to the present invention, a metal bump 805 made of gold (Au), silver (Ag), palladium (Pd), aluminum (Al) or copper (Cu) as the first kind of metal is formed on an electrode pad 803 of a semiconductor chip 802, and a lead frame 807 having a fine wire lead 806 of a two-layered structure in which a gold (Au) layer as the second kind of metal is disposed as a lower layer 806a at the lower end face is bonded with the metal bump 805.

A lead frame 807 having a fine wire lead 806 of a two-layered structure in which a gold (Au) layer 806a is disposed

as the second kind of metal on the lower layer surface, and an upper layer 806b is constituted with copper (Cu) is bonded with the metal bump 805.

Fig. 16 is a schematic cross sectional view of a ninth embodiment of a semiconductor device according to the present invention.

As shown in the figure, in a semiconductor device 901 according to the present invention, a metal bump 905 made of gold (Au), silver (Ag), palladium (Pd), aluminum (Al) or copper (Cu) as the first kind of metal is formed on an electrode pad 903 of a semiconductor chip 902.

A lead frame 907 having a fine wire lead 906 of a two-layered structure in which a silver (Ag) layer 906a is disposed as the second kind of metal on the lower layer surface, and an upper layer 906b is constituted with copper (Cu) is bonded with the metal bump 905.

Fig. 17 is a schematic cross sectional view of a tenth embodiment of a semiconductor device according to the present invention.

As shown in the figure, in a semiconductor device 1001 according to the present invention, a metal bump 1005 made of gold (Au), silver (Ag), palladium (Pd), aluminum (Al) or copper (Cu) as the first kind of metal is formed on an electrode pad 1003 of a semiconductor chip 1002.

A lead frame 1007 having a fine wire lead 1006 of a two-layered structure in which a palladium (Pd) layer 1006a is disposed as the second kind of metal on the lower layer surface, and an upper layer 1006b is constituted with copper (Cu) is bonded with the metal bump 1005.

The feature of the operation of each of the semiconductor devices from the second to the tenth embodiments is substantially identical with that in the first embodiment.

Fig. 18 and Fig. 19 are explanatory views for respective steps in the first embodiment of the method of manufacturing the semiconductor device according to the present invention.

In the first embodiment of the method of manufacturing the semiconductor device according to the present invention, a metal bump 183 made of a first kind of metal is formed on an electrode pad 182 of a semiconductor chip 180 using a bump bonder 181 or the like as shown in Fig. 18 as a first step.

In this case, a silicon chip, as well as a chip made of a compound semiconductor such as GaAs, GaP or GaN are applied as the semiconductor chip 180. In this preferred embodiment, a silicon chip is applied as an example.

In the same manner, as the metal bump 183, a gold (Au) bump, silver (Ag) bump, palladium (Pd) bump, aluminum (Al)

bump, copper (Cu) bump or the like is applied as the first kind of metal as described above. In this preferred embodiment, a gold metal bump is applied as an example.

When the palladium (Pd) bump, aluminum (Al) or copper (Cu) is applied it is preferably conducted under a reducing atmosphere.

In Fig. 18, the gold (Au) bump 183 is formed as a connection electrode for the aluminum electrode pad 182 of the silicon chip 180 by applying ultrasonic waves US using a ultrasonic type bump bonder 181.

As the forming condition, a gold wire of 25 μm wire diameter is used, and ultrasonic waves US at a frequency of 60 kHz to 200 kHz and an output of 10 mW to 50 mW are applied for 10 msec to 50 msec, to form the gold bump 183 with 45 μm of ball diameter.

A pressure of 50 g is applied per each bump for several seconds to conduct planarization to the gold bump 183 formed as described above. In this way, formation of the gold bump 183 on the aluminum electrode pad 182 is completed.

In the next step, as shown in Fig. 19, the electrode pad 182 and a lead frame 185 of a multilayered structure which is partially metal plated with a second kind of metal M2 are bonded by applying ultrasonic waves US under heating H and pressurization P.

A lower end face of a fine wire lead (constituted with the second kind of metal) 185a of the lead frame 185 of the multilayered structure is abutted against the metal bump (constituted with the first kind of metal M1) 183, and a fine wire lead portion of the lead frame 185 is bonded to the gold bump 183 by using an ultrasonic single point bonder 190.

As examples of the bonding conditions, ultrasonic waves US at a frequency from 60 kHz to 200 kHz and at an output from 10 mW to 100 mW are applied for 10 msec to 50 msec under heating at 100°C to 200 °C as a temperature (H) while applying a pressure (P) of 50 g to 200 g to the top end portion of the lead frame.

Alternatively, bonding may be attained without applying ultrasonic waves but by applying pressure and heating to both of the lead frame and the gold bump. For example, it can be conducted by applying a pressure of 50 g to 250 g for 5 sec to 15 sec per each bump at a heating temperature of 100°C to 500°C. According to the bonding conditions, all the lead frames and the gold bumps can be bonded at once by pressurization for once, by which productivity can be improved.

Further, if the first kind of the metal M1 and the second kind of the metal M2 are made of an identical metal, the bonding portion between the gold bump and the lead frame

can be enhanced for compatibility during melting, thereby enabling to obtain bonding of high bonding accuracy and high quality.

Further, since satisfactory bonding is difficult if oxide layers or organics are formed on the lower end face of the multilayered lead frame, it is preferred to apply a step of sputtering a lead frame bonding surface with plasmas such as of an argon gas or hydrogen thereby removing oxide layers or organics formed on the bonding surface of the lead frame prior to the bonding of the lead frame to the metal bump. The removing step can improve the bondability.

As described above, according to the present invention, since a ball-like gold (Au) bump is formed, and a lead frame of a multilayered structure is bonded with an aluminum electrode pad of a semiconductor chip impact shocks such as pressure or ultrasonic vibrations applied upon bonding are absorbed or attenuated by the gold bump to moderate undesired effects.

The shock moderation can suppress occurrence of disadvantages such as injury formed to a portion below the electrode pad of the semiconductor chip, crackings to the interlayer film between the electrode pad and the silicon substrate, to cause electric leakage between the electrode pad or silicon, or partial breakage of the silicon substrate

to result in peeling of the bonded portion, thereby enabling to attain a semiconductor device having stable operation and high reliability.

As has been described above specifically, since the method of manufacturing the semiconductor device according to claim 1 of the present invention comprises a step of forming the metal bump of the first kind of metal on the electrode pad of the semiconductor chip, and a step of bonding, by way of the metal bump, the electrode pad and the lead frame of the multilayered structure partially metal plated with the second kind of metal at least by heating and pressurization, the metal bump absorbs vibrations to provide an effect capable of avoiding occurrence of injury in the semiconductor chip which was liable to occur to a portion below the electrode pad.

Further, since the bonding operation comprises heating and pressurization with no vibration or the like, impact shocks are not applied on the semiconductor chip or the electrode pad thereof, so that displacement of the lead is not caused during bonding operation and the bonding accuracy can be improved. This can provide satisfactory bonding even for a semiconductor chip with a narrow electrode pad pitch.

In addition to the foregoings, since all the leads can be bonded at once, the productivity is improved.

Since the method of manufacturing the semiconductor device according to claim 2 of the present invention has a constitution in which the bonding is conducted by applying heating and pressurization in claim 1, more efficient bonding is possible by the addition of ultrasonic energy.

Since the method of manufacturing the semiconductor device according to claim 3 of the present invention, the first kind of the metal and the second kind of the metal are made of an identical metal in claim 1, the bonded portion between the metal bump and the lead frame has excellent compatibility upon melting, so that bonding at high bonding accuracy and high quality is possible.

Since the method of manufacturing the semiconductor device according to claim 4 of the present invention, the first kind of the metal and the second kind of the metal are made of an identical metal in claim 1, the bonded portion between the metal bump and the lead frame has excellent compatibility upon melting, so that bonding at high bonding accuracy and high quality is possible at high efficiency also by the effect of ultrasonic waves.

Since the method of manufacturing the semiconductor device according to the claim 5 of the present invention comprises a step of treating at least the surface of the bonded portion of the lead frame by plasma irradiation prior

to bonding of the lead frame with the metal bump in claim 1, contaminants deposited on the surface and would otherwise result in the troubles in bonding can be removed, thereby enabling bonding at good quality.

In the semiconductor device according to claim 6 of the present invention, since the metal bump made of the first kind of metal is formed on the electrode pad of the semiconductor chip, and the lead frame of the multilayered structure having the second kind of metal disposed on the surface thereof is bonded with the metal bump, thermal or mechanical impact shocks transmitted from the outside of the semiconductor device by way of the lead frame, for example, upon assembling to the printed circuit substrate or during operation after assembling are absorbed or attenuated in the metal bump, by which undesired effects of the impact shocks on the electrode pad or the semiconductor chip can be moderated thereby attaining stable operation and extended working life.

Further, in the semiconductor device according to claim 7 of the present invention, since the first kind of metal and the second kind of metal are constituted as an identical metal, the bonded portion between the metal bump and the lead frame is excellent in the compatibility upon melting, to provide bonding at high accuracy and good quality

thereby attaining stable operation and extended working life.



What is claimed is:

1. A method of manufacturing a semiconductor device comprising the steps of:

forming a metal bump of a first kind of metal on an electrode pad of a semiconductor chip; and

bonding said electrode pad and a lead frame of a multilayered structure partially metal plated with a second kind of metal by way of the metal bump at least by heating and pressurization.

2. A method of manufacturing a semiconductor device as claimed in claim 1, wherein said bonding is conducted by applying heating and pressurization, and ultrasonic waves.

3. A method of manufacturing a semiconductor device as claimed in claim 1, wherein said first kind of the metal and said second kind of the metal are made of an identical metal.

4. A method of manufacturing a semiconductor device as claimed in claim 2, wherein said first kind of the metal and said second kind of the metal are made of an identical metal.

5. A method of manufacturing a semiconductor device as claimed in claim 1 characterized by comprising a step of treating at least the surface of the bonding portion of said lead frame with plasma irradiation prior to bonding of said lead frame to said metal bump.

6. A semiconductor device wherein a metal bump with a



first kind of metal is formed on an electrode pad of a semiconductor chip, and a lead frame of a multilayered structure having a second kind of metal disposed on the surface thereof is bonded with the metal bump.

7. A semiconductor device as claimed in claim 6, wherein said first kind of metal and said second kind of metal are of an identical metal.