A SEMICONDUCTOR DEVICE

Field of the Invention

This invention relates to a semiconductor device and more particularly, but not exclusively, concerns a VD (vertical diffusion) MOS device for use in RF (radio frequency) power applications for example.

Background of the Invention

A particular kind of semiconductor device, known in the art as a VDMOSFET, has been identified as being particularly useful for broadband radio frequency (RF) applications due to its high reliability and due to the existence of well tried and tested fabrication technology appropriate to its manufacture (see H. Esaki and O. Ishikawa, "A 900 MKz, VD-MOSFET with silicide gate self-aligned channel", International Electron Devices Meeting Digest, Abstract 16.6 pp.447-449 (1984)). VD MOS devices dominate high power RF applications thanks to their high voltage capability. As compared to RF LD (lateral diffusion) MOSFETs, which are used in high frequency, narrow band applications where higher gain is needed, VDMOSFET devices are however known to exhibit a lower frequency capability due to their high parasitic feedback capacitance (C_{rss}) between gate and drain (see M. Trivedi, P. Khandelwal and K. Shenai, "Performance modeling of Power MOSFETS", IEEE Trans. Electron Devices, Vol-46, pp.1794-1802 (1999), and M. Trivedi and K. Shenai, "Comparison of RF performance of vertical and lateral DMOSFET", IEEE

ISPSD 1999, pp.245-248). In order to reduce the parasitic feedback capacitance (C_{rss}), it has been proposed to split the unitary gate structure of the originally proposed VDMOSFET devices so that the gate comprises separate structures each of which covers just one channel region in the VDMOS structure. The resultant split gate structure, as will be explained more fully hereinafter, has the definite advantage of exhibiting a reduction in C_{rss} because the overlap capacitance (C_{ox}) between the gate and the substrate is reduced (see the abovementioned Esaki and Ishikawa reference). However, the modified split gate structure gives rise to two drawbacks, namely: (1) the split gate structure suffers from a lower breakdown voltage due to high electric field crowding on the substrate surface under the gate ends, and (2) the substrate depletion capacitance (C_{si}) between gate and drain is large, because there is less depletion in the substrate. Since the parasitic feedback capacitance (C_{rss}) is a function of the sum of the overlap capacitance (C_{ox}) and the substrate depletion capacitance (C_{si}), the net result is that C_{rss} is not so much improved.

Objects and Summary of the Invention

The principal object of the present invention is to overcome or at least substantially reduce some at least of the above-mentioned drawbacks.

It is an object of the present invention also to provide a semiconductor device which is efficient and reliable for application as a radio frequency power device and which is capable of achieving one or more of a low parasitic feedback

capacitance, a high breakdown voltage, a low channel resistance and a high transconductance in a controllable manner.

In broad terms, the present invention resides in the concept of taking advantage of the aforementioned split gate proposal to reduce the gate overlap capacitance C_{ox} and restoring substrate depletion to achieve a low substrate depletion capacitance C_{si} by provision of an electrode between the spaced apart gate electrodes and appropriately biassing such electrode, for example by connecting it to the source, during operation of the device. With a low C_{ox} and a low C_{si}, the feedback capacitance can be correspondingly low.

In accordance with an exemplary embodiment of the invention which will be described hereafter in detail, a VDMOSFET device has spaced apart sources on one face and a drain on the opposite face of a semiconductor body. Between the spaced apart sources there are provided spaced apart gate structures, and between the spaced apart gate structures there is provided an additional electrode which, in operate of the device, is connected to source. The split gate structure achieves a reduced gate overlap capacitance, just as in the prior art proposal hereinbefore described, and the additional electrode effects depletion of the underlying part of the semiconductor body and reduces the C_{si} component of the feedback capacitance. With a reduced C_{ox} and a reduced C_{si}, the feedback capacitance C_{rss} is much reduced and the high frequency capability of the device correspondingly enhanced.

In addition to exhibiting an enhanced high frequency capability, an additional advantageous effect is achieved by the invention in that the high

electric fields caused by current crowding in the prior art split gate device are significantly reduced so that the device exhibits improved voltage breakdown levels.

The feedback capacitance C_{rss} of the hereinafter described embodiment is also relatively strongly dependent on bias conditions which is significant in regard to improving the efficiency, power gain and output power of the device.

The above and further features of the invention are set forth with particularity in the appended claims and will be described hereinafter with reference to the accompanying drawings.

Brief Description of the Drawings

Figure 1 shows a prior art VDMOS device having a unitary gate structure;

Figure 2 shows another prior art VDMOS device having a split gate structure between the spaced-apart split gates;

Figure 3 shows an exemplary embodiment of the present invention comprising a VDMOS device as in Figure 2 further including a dummy gate structure;

Figure 4 shows simulated electron-hole concentration contours and current flow lines in a prior art split gate VDMOS device as shown in Figure 2;

Figure 5 shows simulated electron-hole concentration contours and current flow lines in a dummy gated VDMOSFET device as shown in Figure 3 and embodying the present invention;

Figure 6 is a graphical simulation showing how feedback capacitance (C_{rss}) varies with drain bias (V_{ds}) in the prior art devices of Figures 1 and 2 and in the device of Figure 3 embodying the present invention;

Figure 7 is a graphical showing of how measured feedback capacitance (C_{rss}) varies with drain bias (V_{ds}) in a prior art device according o Figure 2 and in a device according to Figure 3 embodying the present invention;

Figure 8 is a simulated graphical showing of how feedback capacitance (C_{rss}) varies with gate bias (V_{gs}) and drain bias (V_{ds}) in the prior art device of Figure 2 and in the device of the present invention shown in Figure 3;

Figures 9A and 9B show simulated equipotential lines in, respectively the prior art device of Figure 2 and the device of the present invention shown in Figure 3, strong electric field crowding at the gate ends being shown in Figure 9A and much reduced field strength at the gate ends being shown in Figure 9B;

Figure 10 shows measured breakdown voltage - drain current characteristics in respect of a prior art device according to Figure 2 and a device according to the present invention as shown in Figure 3;

Figure 11 shows measured transfer current-voltage characteristics in respect of a prior art device according to Figure 2 and a device according to the present invention as shown in Figure 3; and

Figure 12 shows measured on-state current-voltage characteristics in respect of a prior art device according to Figure 2 and a device according to the present invention as shown in Figure 3.

Detailed Description of the Embodiments

A conventional VDMOS structure, as originally proposed and as well known, is schematically illustrated in Figure 1. As shown, the device generally indicated by 1, comprises an N- silicon semiconductor body 2, having a unitary gate 3 and two spaced-apart sources 4, 5 at its upper surface 11 and a drain 6 at its lower surface 12. The sources 4, 5 couple to respective N+ regions 7 located within P- type bodies 8 formed in the N- silicon body which is an epitaxial layer formed on an N+ substrate. As is also well known in the art, the amount of capacitive coupling between the gate and the drain limits the high frequency capability of the device such that that the device of Figure 1 operates at a lower frequency capability than conventional RF LDMOSFET devices. The high frequency capability of a VDMOS device is a function of its feedback capacitance (C_{rss}) which, in turn, depends upon two factors, namely the gate-substrate overlap capacitance (C_{ox}) and the silicon substrate depletion capacitance (C_{si}). The feedback capacitance C_{rss} can be described as:

$$C_{rss} = \frac{C_{ox} * C_{si}}{C_{ox} + C_{si}}$$

The overlap capacitance C_{ox} is determined by the gate/substrate overlap area and the thickness of the gate oxide insulation, while the substrate depletion capacitance C_{si} is related to the doping concentration of the silicon body. C_{ox} is substantially constant but C_{si} changes with drain bias. To get a low C_{rss}, both C_{ox} and C_{si} must be minimised. With increasing drain bias, C_{si} decreases due to the substrate depletion caused by reverse biasing of its p-body junction and the

influence of the gate. This makes C_{rss} decrease very quickly with increased drain bias. Due to the high gate/substrate overlap area, however, C_{ox} in the conventional low frequency VDMOS of Figure 1 is very large.

Figure 2 uses the same reference numerals as were used to designate same/like parts in the description of Figure 1 and shows another VDMOS structure 10 which is similar to the structure of Figure 1, the difference being that the gate region is split to form two separate gate portions 3 and 3' at the upper surface 11 which just cover the channel, that is to say the gate is truncated beyond the p-body diffusion edges to minimise gate-drain overlap capacitance for improved RF performance. The split gate structure of Figure 2 exhibits a definite advantage over the Figure 1 structure in that its associated gate overlap capacitance C_{ox} is reduced. However, since the substrate 2 depletes only around the p-body junctions and there is no depletion between the points B_1 and B_2 shown in the Figure, the substrate depletion capacitance C_{si} associated with the split gate structure is disadvantageously large in comparison to that of the Figure 1 structure. The result of this is that the feedback capacitance C_{rss} is not reduced correspondingly with the reduction of C_{ox}. Another, serious drawback of the Figure 2 structure is that the interrupted gate structure unavoidably leads to electric field crowding at the gate ends which causes the breakdown voltage of the device 10 to be reduced.

Figure 3 illustrates an improved VDMOS device structure according to the present invention. Figure 3 uses the same reference numerals as were used to designate same/like parts in the description of Figures 1 and 2. The arrangement,

generally indicated by 20, is the same as that of Figure 2 except that there is an additional electrode 3'', hereinafter referred to as a dummy gate, between the split gate electrodes 3 and 3', the dummy gate 3'' extending just beyond the points B_1 and B_2 shown in the Figure and having its ends spaced apart from the adjoining ends of respective ones of the gates 3,3' by a distance of the order of 1μm.

The device 20 shown in Figure 3 advantageously provides both a reduced gate-drain overlap capacitance C_{ox} and a reduced substrate capacitance C_{si}. In operation, the centrally-positioned dummy gate region 3'' may be shorted to source so that, when a positive drain bias is applied to the device, charge carriers are caused to be depleted in the substrate body 2, not only around the p-bodies but also in the centre of the substrate. This reduces the substrate capacitance C_{si} leading to a fast decrease of the feedback capacitance C_{rss} with drain bias. Because the two gate portions 3 and 3' function in the same way as those of the split gate structure of Figure 2, the overlap capacitance C_{ox} characteristic of the device 20 is as low as that in the split gate structure. Further, because both C_{ox} and C_{si} are effectively reduced, the feedback capacitance characteristic C_{rss} of the device 20 is reduced to a much lower level than in the Figure 2 device. Moreover, when the device 20 is in its off-state with Vgs zero and the drain having to support a high voltage, the dummy gate protects the active gate ends from electric field crowding, as will be more fully described hereinafter, leading to a lower electric field at the gate ends and to a correspondingly high breakdown voltage in the device 20.

The device of Figure 3 may be fabricated employing conventional and well known semiconductor device fabrication techniques. For example, an N+ silicon substrate formed with an N- epitaxial layer has a MOSFET fabrication region defined on the surface of its N- layer by formation of spaced apart silicon oxide layers. Within this region a gate oxide layer is formed and spaced-apart gate electrodes and an intermediate dummy gate electrode are formed on the gate oxide layer. By ion implantation of suitable dopants followed by thermal diffusion, P- type bodies are then formed under the two spaced-apart gate electrodes and extending to the edges of the MOSFET fabrication region. N+ source regions are then formed in the P- type bodies, and the gate oxide layer is selectively removed to permit the formation of source electrodes on the N+ regions. The drain electrode may then be provided on the opposite side of the device.

Figure 4 shows simulated electron hole concentration contours and current flow lines under 5V-gate bias and 28V-drain bias in the Figure 2 VDMOSFET with a split gate structure. It can be seen that only the area around the p-bodies are depleted of carriers. There is no depletion in the centre of the substrate. Figure 5 shows simulated depletion contours and current flow lines in the dummy gated VDMOS of Figure 3 under the same bias conditions. In contrast to the split gate VDMOSFET structure of Figure 2, in the dummy gated VDMOSFET structure of Figure 3, the substrate depletes not only around the p-bodies, but also around the whole centre of the substrate, leading to a low C_{si}. Thus, both C_{ox} and

C_{si} are minimised in the dummy gate structure, as previously discussed hereinabove.

Figure 6 shows simulated C_{rss} vs. Vds characteristics for the three structures of Figures 1, 2 and 3. For the conventional structure of Figure 1, C_{rss} at zero bias is relatively large. This is attributed to a large C_{ox}. With increasing drain bias, C_{rss} decreases very quickly in the Figure 1 structure due to strong depletion in the substrate. Compared to the conventional VDMOS of Figure 1, the split gate VDMOS of Figure 2 exhibits a much lower C_{ox}, but C_{rss} decreases in the Figure 2 structure at a much slower rate with increasing drain bias than in the Figure 1 structure due to the silicon substrate undergoing less depletion so that C_{si} is greater. For the dummy gated VDMOS of Figure 3, C_{rss} at zero bias is comparatively low, as in the Figure 2 device, since the active gate area is reduced so as to result a small C_{ox} and moreover, in contrast to the split gate VDMOS of Figure 2, C_{rss} of the dummy gated structure decreases very quickly with increasing drain bias, thereby achieving the smallest C_{rss} of the three structures, since C_{si} is reduced as a result of the increased substrate depletion caused by provision of dummy gate 3''.

Measured C_{rss} curves at Vgs=OV are shown in Figure 7. 500MHz-30W devices were fabricated according to the split gate and dummy gate structures of Figures 2 and 3 respectively using standard RF VDMOS process technology which is well known and need not be described here. The spacing between the active gates and dummy gate was 1μm. Both devices exhibited almost the same C_{rss} at zero drain bias, because C_{ox} is the same and C_{si} at zero bias is almost the

same for both devices. However, with increasing drain bias (V_{ds}), the two devices behaved very differently. For the split gate structure, C_{rss} decreased very gently. At 5V-drain bias, C_{rss} was 4.5pF. Even with 28V drain bias, C_{rss} was still as high as 3.2pF. In contrast to this, C_{rss} in the dummy gated VDMOS device decreased much more quickly. At 5V-drain bias, it reduced to only 1.8pF. It further dropped to as low as 1.1pF at 28V-drain bias, thereby achieving a three fold improvement as compared to the Figure 2 split gate structure. This benefits the RF performance of the device very significantly.

The C_{rss} characteristic in the on-state for the conventional split gate VDMOS and the dummy gated VDMOS devices of Figures 2 and 3 respectively were also investigated using simulation. Figure 8 shows the simulated C_{rss} vs. Vgs characteristics for split gate 30 and dummy gate 31 structures at Vds=2V and Vds=28V, respectively. It can be seen that for any given bias point, the dummy gated VDMOSFET showed a significantly lower C_{rss} than the conventional split gate VDMOSFET.

It can also be seen from Figure 8 that C_{rss} changes dramatically with different Vds~Vgs bias conditions. With Vds=2V, the substrate depletes lightly, C_{si} is large and C_{rss} is strongly influenced by C_{ox} which changes significantly with different gate bias conditions according to whether the device is operating in a sub-threshold region, a linear region or a saturated region. At 28V drain bias, the substrate depletes deeply, C_{si} becomes very small and variation of gate bias has little influence on C_{rss}. It is clear from Figure 8 that, because the dummy gate structure induces full depletion of the substrate, C_{rss} in the dummy gated VDMOS

is much lower than that in the split gate VDMOS and not only is this the case at low drain bias but also it is the case at high drain bias. At the Vgs=10V and Vds=28V operation point for example, C_{rss} is 1.2fF/μm in the split gate structure and is only 0.4fF/μm in the dummy gate structure. A low feedback capacitance C_{rss} is very important for RF circuit design.

In addition to low feedback capacitance, the dummy gated VDMOS of the invention also achieves a higher breakdown voltage and higher reliability. In this connection, Figure 9a shows simulated equipotential lines for the split gate VDMOS structure of Figure 2 and it can be seen that the potential lines are unevenly vertically distributed around the gates. There is sharp electric field crowding at the gate edges, causing a low breakdown voltage. In contrast to this, as can be seen from Figure 9b, equipotential lines for the dummy gated VDMOS structure of Figure 3 are parallel and uniformly distributed under the gates. Thus, the electric field crowding effect is significantly diminished in the dummy gated VDMOS device of the invention, ensuring a higher breakdown voltage.

Measurement results in respect of the breakdown voltage characteristics for the split gate and dummy gated structures of Figures 2 and 3 respectively are shown in Figure 10. The breakdown voltage was only 78V for the split gate VDMOS device, and was improved to more than 100V for the dummy gated VDMOS.

The dummy gate structure proposed by the present invention thus reduces the electric field in the channel regions as can be seen in Figure 9b. It improves the channel length modulation. This allows the channel length to be reduced

without suffering significant short channel degradation, thus achieving a higher transconductance Gm. This is shown in Figure 11 which shows measured transfer characteristics for the split gate and dummy gated structures. Owing to the abovementioned beneficial short channel capability, the on-state resistance of the dummy gate structure can also be significantly reduced. In this connection, Figure 12 shows measured on-state characteristics of the conventional split gate structure of Figure 2 and of the short channel dummy gated structure of Figure 3. As shown in Figure 12, for the same current level the on-state voltage drop was 5.5V for the split gate device and reduced to only 2.3V for the dummy gated device of the invention. This improves the efficiency, power gain and output power of the device. Not only does the dummy gated device of the invention have an improved high frequency capability, therefore, it also has these significant additional attributes.

Having described the invention by reference to a specific embodiment, it is to be well understood that the embodiment is exemplary only and that modifications and variations thereto will occur to those possessed of appropriate skills without departure from the spirit and scope of the present invention as set forth in the appended claims. For example, whereas the described embodiment of the invention has three gates, namely two spaced apart active gates and a central dummy gate, and two spaced apart sources arranged outside of the gates, the same or a similar technical effect could be obtained in alternative VDMOS structures. For example, where a central source is provided between two spaced apart active gates, the advantages of the invention could be obtained by provision

of dummy gates outside of the active gates but still overlying the drain region. The invention can be applied to any VDMOS structure so long as the dummy gate is designed to overly the drain region.

CLAIMS:

1. A VDMOS device having source, gate and drain electrodes and wherein a further electrode is provided which, in operation of the device, has the effect of enhancing the high frequency capability of the device.

2. A VDMOS device as claimed in claim 1 having spaced apart gate electrodes for reduced gate overlap capacitance.

3. A VDMOS device as claimed in claim 2 wherein said further electrode is located between and spaced apart from both of said gate electrodes.

4. A VDMOS device as claimed in claim 2 or 3 having spaced apart source electrodes.

5. A VDMOS device as claimed in claim 4 wherein said spaced apart source electrodes are located outside of said spaced apart gate electrodes.

6. A VDMOS device as claimed in any preceding claim wherein said further electrode is connected to said source electrode(s).

* C L M S *

7. A VDMOS device as claimed in any preceding claim wherein said further electrode is arranged to reduce current crowding in operation of the device.

8. A method of manufacturing a VDMOS device, wherein an electrode is provided in the device in addition to the source, gate and drain electrodes, said additional electrode being arranged in the device to enhance its high frequency operating capability.

9. A method as claimed in claim 8 wherein said additional electrode is produced with said gate electrode.

10. A semiconductor device comprising a semiconductor body having electrodes spaced on opposite sides thereof for current flow therebetween in dependence upon a control signal from a control electrode, and wherein means are additionally provided for inducing carrier depletion in the semiconductor body so as to reduce the capacitance of the device and enhance its high frequency capability.

11. A semiconductor device as claimed in claim 10 configured as a field effect transistor.

* C L M S *

12. A semiconductor device as claimed in claim 11 wherein source and gate electrodes are provided on one side of said semiconductor body and a drain electrode is provided on the opposite side of said semiconductor body.

13. A semiconductor device as claimed in claim 12 wherein there are spaced apart gate electrodes and said means for inducing carrier depletion comprises a further electrode between said gate electrodes.

14. A semiconductor device as claimed in claim 13 wherein spaced apart source electrodes are provided on opposite sides of said spaced apart gate electrodes.

15. A VDMOSFET split gate device having a further electrode between the gate electrodes.

16. A method of enhancing the high frequency response of a VDMOS device comprising providing an additional electrode in the device for causing depletion in the semiconductor body of the device.

