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THIS SHEET HAS BEEN
REPLACED

MICROCOMPUTER SYSTEM EMPLOYING ADDRESS OFFSET MECHANISM
TO INCREASE THE SUPPORTED CACHE MEMORY CAPACITY

ABSTRACT

The capacity of cache memory supported by a cache controller can be increased by offsetting the relationship between CPU address output terminals and address input terminals of the cache controller and correspondingly doubling the cache line size. In some cases, additional logic generates a hidden memory cycle so as to fetch from memory that number of bytes equal to the new line size regardless of the width of the data bus. The hidden memory cycle is initiated by a read miss and further logic generates a memory address which is not generated by the CPU. The hidden memory cycle is maintained transparent to the CPU and cache controller by inhibiting the change in a READY signal until completion of both the normal memory cycle and the hidden memory cycle.