

ABSTRACT

It is an object of the present invention to provide a technology of a semiconductor integrated circuitry that allows each of the DRAM memory cells to be divided finely so as to be more highly integrated and operated faster. In a method for manufacturing such a semiconductor integrated circuitry of the present invention, at first, gate electrodes 7 are formed via a gate insulating film 6 on the main surface of a semiconductor substrate 1, and on side surfaces of each of the gate electrodes is formed the first side wall spacer 14 composed of silicon nitride and the second side wall spacer 15 composed of silicon oxide. Then, in the selecting MISFET Qs in the DRAM memory cell area are opened connecting holes 19 and 21 in a self-matching manner with respect to the first side wall spacers 14 and are formed connecting portion connecting a conductor 20 to a bit line BL. In addition, in the N channel MISFETs Qn1 and Qn2, and in the P channel MISFET Qp1 in areas other than the DRAM memory cell area are formed high density N-type semiconductor areas 16 and 16b, as well as a high density P-type semiconductor area 17 in a self-matching manner with respect to the second side wall spacers 15.

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