commonly coupled to the interconnect M1-2 via the sub-select gate lines SGD2a through SGD2d are included in the string unit SU2. The memory pillars MP commonly coupled to the interconnect M1-3 via the sub-select gate lines SGD3a through SGD3d are included in the string unit SU3.

Each of the current path selection portions CNL extends in a direction different from the X direction in an XY plane above the memory pillar MP. Each of the current path selection portions CNL is arranged to intersect the memory pillars MP respectively arranged in the rows adjacent to each other. In the drawings referred to below, directions in which the current path selection portions CNL extend in the XY plane are defined as a P direction and a Q direction. That is, the P direction and the Q direction are directions intersecting the X direction and parallel to the XY plane.

In the example of FIG. 3, each of the current path selection portions CNL is arranged so as to intersect a total of two memory pillars MP respectively arranged in the two adjacent rows. Specifically, the current path selection portion CNL arranged to intersect the memory pillar MP arranged in the i-th row and the memory pillar MP arranged in the (i+1)-th row extends in the P direction (i = 1, 5, 9, and 13). The current path selection portion CNL arranged to intersect the memory pillar MP arranged in the j-th rows and the memory pillar MP arranged in the (j+1)-th row extends in the Q direction (j = 3, 7, 11, and 15). In a

example, the upper end of the core film 30 is located above the uppermost conductive layer 23. The lower end of the core film 30 is located above the conductive layer 21. The semiconductor film 31 surrounds the core film 30. A portion of the semiconductor film 31 is in contact with the conductive layer 21 in a lower portion of the memory pillar MP. The stacked film 32 covers the side surface and the bottom surface of the semiconductor film 31 excluding a portion where the semiconductor film 31 and the conductive layer 21 are in contact. The upper end of the stacked film 32 is aligned with the upper end of the semiconductor film 31. The core film 30 contains, for example, an insulator made of silicon oxide, etc. The semiconductor film 31 contains, for example, silicon.

The conductive film 33 includes a portion extending in the Z direction and a portion extending in the X direction. The portion of the conductive film 33 extending in the Z direction functions as a pillar-shaped electrode SP. The portion of the conductive film 33 extending in the X direction functions as one of the sub-select gate lines SGD0a to SGD3d. In the illustrated region, four conductive films 33 respectively including portions functioning as the sub-select gate lines SGD2c, SGD3c, SGD2d, and SGD3d are indicated. The lower end of the portion of the conductive film 33 extending in the Z direction is not in contact with the upper end of the semiconductor film 31. The upper end of the portion of the conductive film 33 extending in the Z

conductive film 33 extending in the X direction, the conductive layer 36, and the insulating layer 37. The insulating layer 37 and the insulating film 38 contain, for example, silicon nitride.

The members SLT include an insulating film 39. The insulating film 39 separates the conductive layers 22 and 23. The lower end of the insulating film 39 reaches the conductive layer 21.

The conductive layer 25 is provided on the upper surface of the portion of the semiconductor film 35 extending in the P direction or the Q direction. The conductive layer 26 is provided on the upper surface of the conductive layer 25. The conductive layers 25 and 26 are used as the contacts CV and VYA, respectively. In the illustrated region, one contact CV and one contact VYA corresponding to the portion of the semiconductor film 35 extending in the P direction are indicated. One conductive layer 24 is provided on the upper surface of the conductive layer 26. The conductive layer 24 functions as the bit line BL.

FIG. 5 is a cross-sectional view taken along line V-V and showing an example of a cross-sectional structure of the memory cell transistor in the semiconductor memory device according to the first embodiment. More specifically, FIG. 5 includes a cross-sectional structure of the memory pillar MP in a layer parallel to the surface of the semiconductor substrate 20 and including the

The conductive layer 25 is provided on the upper surface of the portion of the semiconductor film 31 extending in the P direction. The conductive layer 26 is provided on the upper surface of the conductive layer 25. The conductive layers 25 and 26 are used as the contacts CV and VYA, respectively. In the illustrated region, one of four sets of contacts CV and VYA corresponding to portions of the semiconductor film 31 extending in the P direction is indicated. One conductive layer 24 is provided on the upper surface of the conductive layer 26. The conductive layer 24 functions as the bit line BL.

FIG. 21 is a cross-sectional view taken along line XXI-XXI and showing an example of a cross-sectional structure of a select transistor in the semiconductor memory device according to the second embodiment. More specifically, FIG. 21 includes a cross-sectional structure of the memory pillar MP in a layer parallel to the surface of the semiconductor substrate 20 and including the conductive layer 27. As shown in FIG. 21, the stacked film 32 includes, for example, a tunnel insulating film 32a, a charge accumulating film 32b, and a block insulating film 32c.

As shown in FIG. 21, the portion of the conductive film 33 extending in the Z direction is provided, for example, in the central portion of the memory pillar MP. The portion of the insulating film 34 extending in the Z direction surrounds the side surface of the portion of the

gate line SGS, the conductive layers 23 respectively functioning as the word lines WL0 through WL7, the conductive layer 27 functioning as the select back gate line BSGDa, and the conductive layer 28 functioning as the select back gate line BSGDb are formed. The slits are filled with the insulating film 39. Thus, the members SLT are formed.

Next, as shown in FIG. 31, a hole H4 is formed in a region where a structure corresponding to the contact CV is to be formed. Specifically, a mask having openings in regions corresponding to the contacts CV is formed by photolithography or the like. Then, a plurality of holes H4 penetrating the insulating layer 50 are formed by anisotropic etching using the mask. In a bottom portion of each hole H4, a part of the upper surface of the insulating layer 37, a part of the side surface of the insulating film 38, and a part of the portion of the semiconductor film 31 extending in the P direction are exposed. For forming the holes H4, anisotropic etching with a large selectivity ratio of silicon oxide to silicon nitride is applied. Thus, the positions of the holes H4 can be self-aligned while suppressing exposure of the conductive film 33 and the conductive layer 36.

Next, as shown in FIG. 32, the contacts CV, VYA, and VYB (not shown) and the bit lines BL are formed. To be specific, the holes H4 are filled with the conductive layer 25. Thereafter, a process of forming the contacts VYA and

layer 24 is provided on the upper surface of the conductive layer 26. The conductive layer 24 functions as the bit line BL.

The conductive film 33 includes a portion extending in the Z direction and a portion extending in the X direction. The portion of the conductive film 33 extending in the Z direction functions as the pillar-shaped electrode SP. The portion of the conductive film 33 extending in the X direction functions as one of the sub-select gate lines SGD0a through SGD3b. Each of the portions extending in the X direction of the seven conductive films 33 functioning as the sub-select gate line SGD0b and SGD1a through SGD3b is shared by the memory pillars MP in two adjacent rows. Each of the portions extending in the X direction of the two conductive films 33 functioning as the sub-select gate lines SGD0a and SGD0c is shared by the memory pillars MP in one row. In the illustrated region, three conductive films 33 including portions functioning as the sub-select gate lines SGD2b, SGD3b, and SGD0c are indicated.

The conductive layer 29 is provided on the upper surface of the portion of the conductive film 33 extending in the X direction. The conductive layer 29 is used as the contact CVB. In the illustrated region, three contacts CVB corresponding to the sub-selection gate lines SGD2b, SGD3b, and SGD0c are indicated.

3.2 Manufacturing Method

Each of FIGS. 35 through 41 is a diagram showing an