CLAIMS

What is claimed is:

1. A semiconductor device assembly comprising:

a substrate including a plurality of conductive terminals disposed on or in a surface thereof;

a first semiconductor die including an active surface and a plurality of bond pads disposed in a first selected connection pattern on or in the active surface;

a second semiconductor die including an active surface and a plurality of bond pads disposed in a second selected connection pattern on or in the active surface of the second semiconductor die, the active surface of the first semiconductor die facing the active surface of the second semiconductor die;

a plurality of conductive structures, each conductive structure of the plurality being electrically and structurally coupled to a bond pad of the first semiconductor die and a bond pad of the second semiconductor die;

a plurality of laterally extending conductive elements, a first end of each laterally extending conductive element being structurally and electrically coupled to a conductive terminal of the substrate, a second end of each laterally extending conductive element being structurally and electrically coupled to at least one of a bond pad of the first semiconductor die, a bond pad of the second semiconductor die, and a conductive structure of the plurality of conductive structures; and

a plurality of discrete dielectric structures disposed between the active surface of the first semiconductor die and the active surface of the second semiconductor die; wherein an intermediate portion of at least one laterally extending conductive element of the plurality of laterally extending conductive elements, between the first end and the second end of the at least one laterally extending conductive element of the plurality, passes through at least one discrete dielectric structure of the plurality of discrete dielectric structures.

2. The semiconductor device assembly of claim 1, wherein the second selected connection pattern is a mirror image of the first selected connection pattern.

3. The semiconductor device assembly of claim 1, wherein the second selected connection pattern is identical to the first selected connection pattern.

4. The semiconductor device assembly of claim 1, wherein each laterally extending conductive element of the plurality comprises a bond wire.

5. The semiconductor device assembly of claim 1, wherein the second end of each laterally extending conductive element is disposed between and structurally and electrically coupled to both a bond pad of the first semiconductor die and a conductive structure.

6. The semiconductor device assembly of claim 1, wherein the plurality of discrete dielectric structures comprises a first discrete piece of tape attached to the active surface of the first semiconductor die and a second discrete piece of tape attached to the first discrete piece of tape, a portion of each laterally extending conductive element passing between the first discrete piece of tape and the second discrete piece of tape.

7. The semiconductor device assembly of claim 6, wherein the first discrete piece of tape and the second discrete piece of tape each comprises one of a strip of dielectric material and a film of dielectric material.

8. The semiconductor device assembly of claim 1, wherein a portion of each laterally extending conductive element passes through at least one dielectric structure, each dielectric structure configured to position the portion of the laterally extending conductive element between the active surface of the first semiconductor die and the active surface of the second semiconductor die to prevent contact between the laterally extending conductive element and the active surface of the first semiconductor die and the active surface of the second semiconductor die.

9. The semiconductor device assembly of claim 1, wherein each dielectric structure of the plurality is disposed proximate a lateral edge of at least one of the first semiconductor die and the second semiconductor die.

10. The semiconductor device assembly of claim 1, wherein each discrete dielectric structure is attached to both the active surface of the first semiconductor die and the active surface of the second semiconductor die.

11. The semiconductor device assembly of claim 1, wherein a portion of only one laterally extending conductive element extends through each discrete dielectric structure.

12. The semiconductor device assembly of claim 1, wherein the plurality of bond pads of the first semiconductor die is disposed substantially along a centerline of the first semiconductor die and the plurality of bond pads of the second semiconductor die is disposed substantially along a centerline of the second semiconductor die.

13. The semiconductor device assembly of claim 1, wherein the plurality of bond pads of the first semiconductor die is disposed proximate a lateral edge of the first semiconductor die and the plurality of bond pads of the second semiconductor die is disposed proximate a lateral edge of the second semiconductor die.

14. The semiconductor device assembly of claim 13, wherein each conductive structure comprises a solder bump.

15. The semiconductor device assembly of claim 1, wherein a back side of the first semiconductor die is attached to the substrate.

16. The semiconductor device assembly of claim 1, wherein the substrate comprises one of a circuit board, an interposer, a semiconductor die, and a semiconductor wafer.

17. The semiconductor device assembly of claim 1, further comprising at least one additional semiconductor die.

18. The semiconductor device assembly of claim 17, wherein the at least one additional semiconductor die comprises:

a third semiconductor die including an active surface and a plurality of bond pads disposed in a third selected connection pattern on or in the active surface;

a fourth semiconductor die including an active surface and a plurality of bond pads disposed in a fourth selected connection pattern on or in the active surface, the active surface of the first additional semiconductor die facing the active surface of the second additional semiconductor die.

19. The semiconductor device assembly of claim 18, further comprising:

an additional plurality of conductive structures, each conductive structure of the additional plurality being electrically and structurally coupled to a bond pad of the third semiconductor die and the fourth semiconductor die; and

an additional plurality of laterally extending conductive elements, each laterally extending conductive element of the additional plurality including a first end structurally and electrically coupled to a conductive terminal of the substrate and a second end structurally and electrically coupled to at least one of a bond pad of the third semiconductor die, a bond pad of the fourth semiconductor die, and a conductive structure of the additional plurality.

20. The semiconductor device assembly of claim 18, wherein a back side of the third semiconductor die is attached to a back side of the second semiconductor die.

21. The semiconductor device assembly of claim 1, further comprising a dielectric encapsulant material substantially enclosing the first semiconductor die and the second semiconductor die.

22. An electronic system comprising:

at least one electronic signal processing device;

at least one memory device configured to communicate electrically with the at least one electronic signal processing device, the at least one memory device comprising a semiconductor device assembly, the semiconductor device assembly comprising:

a substrate including a plurality of conductive terminals disposed on or in a surface thereof;

a first semiconductor die including an active surface and a plurality of bond pads disposed in a first selected connection pattern on or in the active surface;

a second semiconductor die including an active surface and a plurality of bond pads disposed in a second selected connection pattern on or in the active surface, the active surface of the first semiconductor die facing the active surface of the second semiconductor die;

a plurality of conductive structures, each conductive structure of the plurality being electrically and structurally coupled to a bond pad of the first semiconductor die and to a bond pad of the second semiconductor die;

a plurality of laterally extending conductive elements, a first end of each laterally extending conductive element being structurally and electrically coupled to a conductive terminal of the substrate, a second end of each laterally extending conductive element being structurally and electrically coupled to at least one of a bond pad of the first semiconductor die, a bond pad of the second semiconductor die, and a conductive structure;

a plurality of discrete dielectric structures disposed between the active surface of the first semiconductor die and the active surface of the second semiconductor die, an intermediate portion of at least one laterally extending conductive element of the plurality of laterally extending conductive elements, between the first end and the second end of the at least one laterally extending conductive element of the plurality, passing through at least one discrete dielectric structure of the plurality of discrete dielectric structures; and

at least one of an input device and an output device configured to communicate electrically with at least one of the memory device and the electronic signal processing device.

23. The electronic system of claim 22, wherein the second selected connection pattern is a mirror image of the first selected connection pattern.

24. The electronic system of claim 22, wherein each laterally extending conductive element of the plurality comprises a bond wire.

25. The electronic system of claim 22, wherein the second end of each laterally extending conductive element is disposed between and structurally and electrically coupled to both a bond pad of the first semiconductor die and a conductive structure.

26. The electronic system of claim 22, wherein a portion of only one laterally extending conductive element extends through each discrete dielectric structure.

27. The electronic system of claim 22, wherein a portion of each laterally extending conductive element passes through at least one dielectric structure, each dielectric structure configured to position the portion of the laterally extending conductive element between the active surface of the first semiconductor die and the active surface of the second semiconductor die to prevent contact between the laterally extending conductive element and the active surface of the first semiconductor die and the active surface of the second semiconductor die.

28. The electronic system of claim 22, wherein each dielectric structure of the plurality is disposed proximate a lateral edge of at least one of the first semiconductor die and the second semiconductor die.

29. The electronic system of claim 22, wherein each discrete dielectric structure is attached to both the active surface of the first semiconductor die and the active surface of the second semiconductor die.

30. The electronic system of claim 22, wherein the plurality of bond pads of the first semiconductor die is disposed substantially along a centerline of the first semiconductor die and the plurality of bond pads of the second semiconductor die is disposed substantially along a centerline of the second semiconductor die.

31. The electronic system of claim 22, wherein the plurality of bond pads of the first semiconductor die is disposed is an array on the active surface of the first semiconductor die and the plurality of bond pads of the second semiconductor die is disposed in an array on the active surface of the second semiconductor die.

32. The electronic system of claim 31, wherein each conductive structure comprises a solder bump.

33. The electronic system of claim 22, wherein a back side of the first semiconductor die is attached to the substrate.

34. The electronic system of claim 22, wherein the substrate comprises a circuit board.

35. The electronic system of claim 22, further comprising at least one additional semiconductor die.

36. The electronic system of claim 35, wherein the at least one additional semiconductor die comprises:

a third semiconductor die including an active surface and a plurality of bond pads disposed in a third selected connection pattern on or in the active surface;

a fourth semiconductor die including an active surface and a plurality of bond pads disposed in a fourth selected connection pattern on or in the active surface, the active surface of the third semiconductor die facing the active surface of the fourth semiconductor die.

37. The electronic system of claim 36, further comprising:

an additional plurality of conductive structures, each conductive structure of the additional plurality being electrically and structurally coupled to a bond pad of the third semiconductor die and the fourth semiconductor die; and

an additional plurality of laterally extending conductive elements, each laterally extending conductive element of the additional plurality including a first end structurally and electrically coupled to a conductive terminal of the substrate and a second end structurally and electrically coupled to at least one of a bond pad of the third semiconductor die, a bond pad of the fourth semiconductor die, and a conductive structure of the additional plurality.

38. The electronic system of claim 36, wherein a back side of the third semiconductor die is attached to a back side of the second semiconductor die.

39. The electronic system of claim 22, further comprising a dielectric encapsulant material substantially enclosing the first semiconductor die and the second semiconductor die.

40. A method of manufacturing a semiconductor device assembly, the method comprising:

attaching a back side of a first semiconductor die to a substrate;

structurally and electrically coupling a first end of each of a plurality of laterally extending conductive elements to one of a plurality of conductive terminals on or in a surface of the substrate;

structurally and electrically coupling a second end of each of the plurality of laterally extending conductive elements to one of a plurality of bond pads on or in an active surface of the first semiconductor die;

structurally and electrically coupling each of a plurality of conductive structures to one of a plurality of bond pads of a second semiconductor die;

aligning at least some conductive structures of the plurality with at least some of the plurality of bond pads of the first semiconductor die, an active surface of the second semiconductor die facing an active surface of the first semiconductor die; and

structurally and electrically coupling the at least some conductive structures of the plurality to the at least some of the plurality of bond pads of the first semiconductor die.

providing a plurality of discrete dielectric structures between the active surface of the first semiconductor die and the active surface of the second semiconductor die, a portion of each laterally extending conductive element passing through at least one dielectric structure.

41. The method of claim 40, wherein structurally and electrically coupling a first end of each of a plurality of laterally extending conductive elements comprises structurally and electrically coupling a first end of each of a plurality of bond wires to one of a plurality of conductive terminals on or in a surface of the substrate, and wherein structurally and

electrically coupling a second end of each of the plurality of laterally extending conductive elements comprises structurally and electrically coupling a second end of each of the plurality of bond wires to one of the plurality of bond pads on or in an active surface of the first semiconductor die.

42. The method of claim 40, further comprising structurally and electrically coupling the second end of each of the plurality of laterally extending conductive elements to one of the plurality of conductive structures.

43. The method of claim 40, wherein providing a plurality of discrete dielectric structures comprises applying a plurality of discrete dielectric structures to the active surface of at least one of the first semiconductor die and the second semiconductor die at a wafer level.

44. The method of claim 40, wherein providing a plurality of discrete dielectric structures comprises providing a plurality of discrete dielectric structures each comprising one of silicone, a silicone-based material, epoxy, and an epoxy-based material.

45. The method of claim 40, wherein providing a plurality of discrete dielectric structures comprises providing a plurality of discrete dielectric structures each comprising a first discrete piece of tape attached to the active surface of the first semiconductor die and a second discrete piece of tape attached to the active surface of the second semiconductor die, a portion of each laterally extending conductive element passing between the first discrete piece of tape and the second discrete piece of tape.

46. The method of claim 45, further comprising at least one of attaching a first discrete piece of tape to the active surface of the first semiconductor die at the wafer level and attaching a second discrete piece of tape to the active surface of the second semiconductor die at the wafer level.

47. The method of claim 40, wherein providing a plurality of discrete dielectric structures comprises positioning each discrete dielectric structure of the plurality proximate a lateral edge of at least one of the first semiconductor die and the second semiconductor die.

48. The method of claim 40, further comprising attaching each discrete dielectric structure to both the active surface of the first semiconductor die and the active surface of the second semiconductor die.

49. The method of claim 40, wherein structurally and electrically coupling each of a plurality of conductive structures to one of a plurality of bond pads of a second semiconductor die comprises structurally and electrically coupling each of a plurality of solder balls to one of the plurality of bond pads of the second semiconductor die.

50. The method of claim 49, wherein structurally and electrically coupling the at least some conductive structures of the plurality to the at least some of the plurality of bond pads of the first semiconductor die comprises reflowing at least some of the solder balls of the plurality.

51. The method of claim 40, wherein attaching a back side of a first semiconductor die to a substrate comprises attaching a back side of the first semiconductor die to a surface of a circuit board.

52. The method of claim 40, further comprising:

attaching a back side of a first additional semiconductor die to a back side of the second semiconductor die;

structurally and electrically coupling a first end of each of an additional plurality of laterally extending conductive elements to one of the plurality of conductive terminals on or in the surface of the substrate;

structurally and electrically coupling a second end of each of the additional plurality of laterally extending conductive elements to one of a plurality of bond pads on or in an active surface of the first additional semiconductor die;

structurally and electrically coupling each of an additional plurality of conductive structures to one of a plurality of bond pads of a second additional semiconductor die;

aligning at least some conductive structures of the additional plurality with at least some of the plurality of bond pads of the first additional semiconductor die, an active surface of the second additional semiconductor die facing an active surface of the first additional semiconductor die; and

structurally and electrically coupling the at least some conductive structures of the additional plurality to the at least some of the plurality of bond pads of the first additional semiconductor die.

53. The method of claim 40, further comprising encapsulating the first semiconductor die and the second semiconductor die with a dielectric encapsulant material.

54. The method of claim 40, wherein attaching a back side of a first semiconductor die to a substrate comprises attaching a plurality of first semiconductor dice to a surface of a single substrate.

55. The method of claim 54, further comprising dicing the single substrate.

CLAIMS

What is claimed is:

1. A semiconductor device assembly comprising:

a substrate including a plurality of conductive terminals disposed on or in a surface thereof;

a first semiconductor die including an active surface and a plurality of bond pads disposed in a first selected connection pattern on or in the active surface;

a second semiconductor die including an active surface and a plurality of bond pads disposed in a second selected connection pattern on or in the active surface of the second semiconductor die, the active surface of the first semiconductor die facing the active surface of the second semiconductor die;

a plurality of conductive structures, each conductive structure of the plurality being electrically and structurally coupled to a bond pad of the first semiconductor die and a bond pad of the second semiconductor die;

a plurality of laterally extending conductive elements, a first end of each laterally extending conductive element being structurally and electrically coupled to a conductive terminal of the substrate, a second end of each laterally extending conductive element being structurally and electrically coupled to at least one of a bond pad of the first semiconductor die, a bond pad of the second semiconductor die, and a conductive structure of the plurality of conductive structures; and

a plurality of discrete dielectric structures disposed between and in contact with each of the active surface of the first semiconductor die and the active surface of the second semiconductor die; wherein an intermediate portion of at least one laterally extending conductive element of the plurality of laterally extending conductive elements, between the first end and the second end of the at least one laterally extending conductive element of the plurality, passes through at least one discrete dielectric structure of the plurality of discrete dielectric structures; wherein each discrete dielectric structure is in physical contact with both the active surface of the first semiconductor die and the active surface of the second semiconductor die.

2. The semiconductor device assembly of claim 1, wherein the second selected connection pattern is a mirror image of the first selected connection pattern.

3. The semiconductor device assembly of claim 1, wherein the second selected connection pattern is identical to the first selected connection pattern.

4. The semiconductor device assembly of claim 1, wherein each laterally extending conductive element of the plurality comprises a bond wire.

5. The semiconductor device assembly of claim 1, wherein the second end of each laterally extending conductive element is disposed between and structurally and electrically coupled to both a bond pad of the first semiconductor die and a conductive structure.

6. The semiconductor device assembly of claim 1, wherein the plurality of discrete dielectric structures comprises a first discrete piece of tape attached to the active surface of the first semiconductor die and a second discrete piece of tape attached to the first discrete piece of tape, a portion of each laterally extending conductive element passing between the first discrete piece of tape and the second discrete piece of tape.

7. The semiconductor device assembly of claim 6, wherein the first discrete piece of tape and the second discrete piece of tape each comprises one of a strip of dielectric material and a film of dielectric material.

8. The semiconductor device assembly of claim 1, wherein a portion of each laterally extending conductive element passes through at least one dielectric structure, each dielectric structure configured to position the portion of the laterally extending conductive element between the active surface of the first semiconductor die and the active surface of the second semiconductor die to prevent contact between the laterally extending conductive element and the active surface of the first semiconductor die and the active surface of the second semiconductor die.

9. The semiconductor device assembly of claim 1, wherein each dielectric structure of the plurality is disposed proximate a lateral edge of at least one of the first semiconductor die and the second semiconductor die.

10. The semiconductor device assembly of claim 1, wherein a portion of only one laterally extending conductive element extends through each discrete dielectric structure.

11. The semiconductor device assembly of claim 1, wherein the plurality of bond pads of the first semiconductor die is disposed substantially along a centerline of the first semiconductor die and the plurality of bond pads of the second semiconductor die is disposed substantially along a centerline of the second semiconductor die.

12. The semiconductor device assembly of claim 1, wherein the plurality of bond pads of the first semiconductor die is disposed proximate a lateral edge of the first semiconductor die and the plurality of bond pads of the second semiconductor die is disposed proximate a lateral edge of the second semiconductor die.

13. The semiconductor device assembly of claim 12, wherein each conductive structure comprises a solder bump.

14. The semiconductor device assembly of claim 1, wherein a back side of the first semiconductor die is attached to the substrate.

15. The semiconductor device assembly of claim 1, wherein the substrate comprises one of a circuit board, an interposer, a semiconductor die, and a semiconductor wafer.

16. The semiconductor device assembly of claim 1, further comprising at least one additional semiconductor die.

17. The semiconductor device assembly of claim 16, wherein the at least one additional semiconductor die comprises:

a third semiconductor die including an active surface and a plurality of bond pads disposed in a third selected connection pattern on or in the active surface;

a fourth semiconductor die including an active surface and a plurality of bond pads disposed in a fourth selected connection pattern on or in the active surface, the active surface of

the first additional semiconductor die facing the active surface of the second additional semiconductor die.

18. The semiconductor device assembly of claim 17, further comprising:

an additional plurality of conductive structures, each conductive structure of the additional plurality being electrically and structurally coupled to a bond pad of the third semiconductor die and the fourth semiconductor die; and

an additional plurality of laterally extending conductive elements, each laterally extending conductive element of the additional plurality including a first end structurally and electrically coupled to a conductive terminal of the substrate and a second end structurally and electrically coupled to at least one of a bond pad of the third semiconductor die, a bond pad of the fourth semiconductor die, and a conductive structure of the additional plurality.

19. The semiconductor device assembly of claim 17, wherein a back side of the third semiconductor die is attached to a back side of the second semiconductor die.

20. The semiconductor device assembly of claim 1, further comprising a dielectric encapsulant material substantially enclosing the first semiconductor die and the second semiconductor die.

21. An electronic system comprising:

at least one electronic signal processing device;

at least one memory device configured to communicate electrically with the at least one electronic signal processing device, the at least one memory device comprising a semiconductor device assembly, the semiconductor device assembly comprising:

a substrate including a plurality of conductive terminals disposed on or in a surface thereof;

a first semiconductor die including an active surface and a plurality of bond pads disposed in a first selected connection pattern on or in the active surface;

a second semiconductor die including an active surface and a plurality of bond pads disposed in a second selected connection pattern on or in the active surface, the active surface of the first semiconductor die facing the active surface of the second semiconductor die;

a plurality of conductive structures, each conductive structure of the plurality being electrically and structurally coupled to a bond pad of the first semiconductor die and to a bond pad of the second semiconductor die;

a plurality of laterally extending conductive elements, a first end of each laterally extending conductive element being structurally and electrically coupled to a conductive terminal of the substrate, a second end of each laterally extending conductive element being structurally and electrically coupled to at least one of a bond pad of the first semiconductor die, a bond pad of the second semiconductor die, and a conductive structure; and

a plurality of discrete dielectric structures disposed between and in contact with each of the active surface of the first semiconductor die and the active surface of the second semiconductor die; wherein an intermediate portion of at least one laterally extending conductive element of the plurality of laterally extending conductive elements, between the first end and the second end of the at least one laterally extending conductive element of the plurality, passes through at least one discrete dielectric structure of the plurality of discrete dielectric structures; wherein each discrete dielectric structure is in physical contact with both the active surface of the first semiconductor die and the active surface of the second semiconductor die; and

at least one of an input device and an output device configured to communicate electrically with at least one of the memory device and the electronic signal processing device.

22. The electronic system of claim 21, wherein the second selected connection pattern is a mirror image of the first selected connection pattern.

23. The electronic system of claim 21, wherein each laterally extending conductive element of the plurality comprises a bond wire.

24. The electronic system of claim 21, wherein the second end of each laterally extending conductive element is disposed between and structurally and electrically coupled to both a bond pad of the first semiconductor die and a conductive structure.

25. The electronic system of claim 21, wherein a portion of only one laterally extending conductive element extends through each discrete dielectric structure.

26. The electronic system of claim 21, wherein a portion of each laterally extending conductive element passes through at least one dielectric structure, each dielectric structure configured to position the portion of the laterally extending conductive element between the active surface of the first semiconductor die and the active surface of the second semiconductor die to prevent contact between the laterally extending conductive element and the active surface of the first semiconductor die and the active surface of the second semiconductor die.

27. The electronic system of claim 21, wherein each dielectric structure of the plurality is disposed proximate a lateral edge of at least one of the first semiconductor die and the second semiconductor die.

28. The electronic system of claim 21, wherein the plurality of bond pads of the first semiconductor die is disposed substantially along a centerline of the first semiconductor die and the plurality of bond pads of the second semiconductor die is disposed substantially along a centerline of the second semiconductor die.

29. The electronic system of claim 21, wherein the plurality of bond pads of the first semiconductor die is disposed is an array on the active surface of the first semiconductor die and the plurality of bond pads of the second semiconductor die is disposed in an array on the active surface of the second semiconductor die.

30. The electronic system of claim 29, wherein each conductive structure comprises a solder bump.

31. The electronic system of claim 21, wherein a back side of the first semiconductor die is attached to the substrate.

32. The electronic system of claim 21, wherein the substrate comprises a circuit board.

33. The electronic system of claim 21, further comprising at least one additional semiconductor die.

34. The electronic system of claim 33, wherein the at least one additional semiconductor die comprises:

a third semiconductor die including an active surface and a plurality of bond pads disposed in a third selected connection pattern on or in the active surface;

a fourth semiconductor die including an active surface and a plurality of bond pads disposed in a fourth selected connection pattern on or in the active surface, the active surface of the third semiconductor die facing the active surface of the fourth semiconductor die.

35. The electronic system of claim 34, further comprising:

an additional plurality of conductive structures, each conductive structure of the additional plurality being electrically and structurally coupled to a bond pad of the third semiconductor die and the fourth semiconductor die; and

an additional plurality of laterally extending conductive elements, each laterally extending conductive element of the additional plurality including a first end structurally and electrically coupled to a conductive terminal of the substrate and a second end structurally and electrically coupled to at least one of a bond pad of the third semiconductor die, a bond pad of the fourth semiconductor die, and a conductive structure of the additional plurality.

36. The electronic system of claim 34, wherein a back side of the third semiconductor die is attached to a back side of the second semiconductor die.

37. The electronic system of claim 21, further comprising a dielectric encapsulant material substantially enclosing the first semiconductor die and the second semiconductor die.

38. A method of manufacturing a semiconductor device assembly, the method comprising:

attaching a back side of a first semiconductor die to a substrate;

structurally and electrically coupling a first end of each of a plurality of laterally extending conductive elements to one of a plurality of conductive terminals on or in a surface of the substrate;

structurally and electrically coupling a second end of each of the plurality of laterally extending conductive elements to one of a plurality of bond pads on or in an active surface of the first semiconductor die;

structurally and electrically coupling each of a plurality of conductive structures to one of a plurality of bond pads of a second semiconductor die;

aligning at least some conductive structures of the plurality with at least some of the plurality of bond pads of the first semiconductor die, an active surface of the second semiconductor die facing an active surface of the first semiconductor die;

structurally and electrically coupling the at least some conductive structures of the plurality to the at least some of the plurality of bond pads of the first semiconductor die;

providing a plurality of discrete dielectric structures between and in contact with the active surface of the first semiconductor die and the active surface of the second semiconductor die, a portion of each laterally extending conductive element passing through at least one dielectric structure; and

attaching each discrete dielectric structure physically to both the active surface of the first semiconductor die and the active surface of the second semiconductor die.

39. The method of claim 38, wherein structurally and electrically coupling a first end of each of a plurality of laterally extending conductive elements comprises structurally and electrically coupling a first end of each of a plurality of bond wires to one of a plurality of conductive terminals on or in a surface of the substrate, and wherein structurally and electrically coupling a second end of each of the plurality of laterally extending conductive elements comprises structurally and electrically coupling a second end of each of the plurality of bond wires to one of the plurality of bond pads on or in an active surface of the first semiconductor die.

40. The method of claim 38, further comprising structurally and electrically coupling the second end of each of the plurality of laterally extending conductive elements to one of the plurality of conductive structures.

41. The method of claim 38, wherein providing a plurality of discrete dielectric structures comprises applying a plurality of discrete dielectric structures to the active surface of at least one of the first semiconductor die and the second semiconductor die at a wafer level.

42. The method of claim 38, wherein providing a plurality of discrete dielectric structures comprises providing a plurality of discrete dielectric structures each comprising one of silicone, a silicone-based material, epoxy, and an epoxy-based material.

43. The method of claim 38, wherein providing a plurality of discrete dielectric structures comprises providing a plurality of discrete dielectric structures each comprising a first discrete piece of tape attached to the active surface of the first semiconductor die and a second discrete piece of tape attached to the active surface of the second semiconductor die, a portion of each laterally extending conductive element passing between the first discrete piece of tape and the second discrete piece of tape.

44. The method of claim 43, further comprising at least one of attaching a first discrete piece of tape to the active surface of the first semiconductor die at the wafer level and attaching a second discrete piece of tape to the active surface of the second semiconductor die at the wafer level.

45. The method of claim 38, wherein providing a plurality of discrete dielectric structures comprises positioning each discrete dielectric structure of the plurality proximate a lateral edge of at least one of the first semiconductor die and the second semiconductor die.

46. The method of claim 38, wherein structurally and electrically coupling each of a plurality of conductive structures to one of a plurality of bond pads of a second semiconductor die comprises structurally and electrically coupling each of a plurality of solder balls to one of the plurality of bond pads of the second semiconductor die.

47. The method of claim 46, wherein structurally and electrically coupling the at least some conductive structures of the plurality to the at least some of the plurality of bond pads of the first semiconductor die comprises reflowing at least some of the solder balls of the plurality.

48. The method of claim 38, wherein attaching a back side of a first semiconductor die to a substrate comprises attaching a back side of the first semiconductor die to a surface of a circuit board.

49. The method of claim 38, further comprising:

attaching a back side of a first additional semiconductor die to a back side of the second semiconductor die;

structurally and electrically coupling a first end of each of an additional plurality of laterally extending conductive elements to one of the plurality of conductive terminals on or in the surface of the substrate;

structurally and electrically coupling a second end of each of the additional plurality of laterally extending conductive elements to one of a plurality of bond pads on or in an active surface of the first additional semiconductor die;

structurally and electrically coupling each of an additional plurality of conductive structures to one of a plurality of bond pads of a second additional semiconductor die;

aligning at least some conductive structures of the additional plurality with at least some of the plurality of bond pads of the first additional semiconductor die, an active surface of the second additional semiconductor die facing an active surface of the first additional semiconductor die; and

structurally and electrically coupling the at least some conductive structures of the additional plurality to the at least some of the plurality of bond pads of the first additional semiconductor die.

50. The method of claim 38, further comprising encapsulating the first semiconductor die and the second semiconductor die with a dielectric encapsulant material.

51. The method of claim 38, wherein attaching a back side of a first semiconductor die to a substrate comprises attaching a plurality of first semiconductor dice to a surface of a single substrate.

52. The method of claim 51, further comprising dicing the single substrate.