FET STRUCTURE USING DISPOSABLE SPACER AND STRESS INDUCING LAYER

Abstract

Some non-limiting example embodiments comprise a disposable spacer formation and removal process and a stress capping layer process. We provide a gate structure over a substrate. We form disposable spacers abutting the at least one gate sidewall. We form S/D regions adjacent the disposable spacers. We remove the disposable spacers. We can form silicide regions over the S/D and gate. In an aspect, we can deposit a stress inducing layer over the gate and surface portions of the substrate adjacent to the gate, wherein the stress inducing liner provides a stress to a portion of the substrate underlying the gate electrode.

Fig. 7B