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PATENT SPECIFICATION

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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Semi-conductor Structure Fabrication

We, TEXAS INSTRUMENTS INCORPORATED, of 6000 Lemmon Avenue, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to hermetically enclosed semiconductor devices and methods of manufacturing same.

In our copending application No. 3633/60, Serial number 945,734, there are described semiconductor networks employing very thin semiconductor wafers. Semiconductor networks are complete circuit configurations formed completely within solid bodies of semiconductive material. The various elements such as resistors, capacitors and amplifying devices of such circuits are fabricated by attaching terminals to the semiconductive body and forming PN junctions at appropriate locations on the semiconductor body and connecting terminals to the semiconductive body so as to utilize the junctions and the semiductive material per se to obtain the desired components. More specifically, the semiconductive material subsisting between two ohmic contacts on the semiconductive body constitutes a resistive element while the capacity across a back-biased PN junction may be employed as a capacitive element. Further, such junctions may be employed as diodes and connections may be made to dual junctions, that is, to PNP or NPN junctions, to form transistor amplifying elements. In the aforesaid copending patent application and divisionals therefrom, various semiconductor networks are discussed and, in particular, a multivibrator and a phase shift oscillator are discussed. In both of these circuits, all of the amplifying elements and capacitors and resistors are formed directly by employing various sections on and junctions in a single semiconductive body.

Semiconductor networks represent a vast advance in the art of circuit miniaturization and although use is made of many of the standard techniques normally employed in the fabrication of semiconductive diodes and transistors, many new techniques of fabrication are also required. For example, in one step in a method for fabricating complete semiconductor network devices or individual transistors or diodes, a semiconductor wafer having a relatively large surface area is first treated uniformly over its entire surface area; that is, when a junction is formed, the junction is formed over one entire surface of the wafer and thereafter the large wafer may be cut into a number of small wafers, all of the same size which may then be mounted and thereafter have further junctions formed thereon or leads connected thereto to form the individual devices. The semiconductor networks thereafter generally require more handling and processing than single transistor or diode devices since several different regions of each small semiconductor wafer for a semiconductor network device must be treated differently whereas for a single transistor or diode device only one, or at the most, two, regions require further treatment. Nevertheless, the semiconductive wafers used to form any device are usually very thin, approximately 0.002 inch thick and are therefore quite delicate and difficult to handle. Further, when the wafers are etched to provide various surface configurations required to form desired circuit components, the wafers become so fragile that they are extremely difficult to handle without their breaking.

[Price 4s. 6d.]

The present invention is a hermetically enclosed semiconductor device including a substrate with substantially flat insulating surface and forming part of an enclosure, a semiconductor body within said enclosure and secured to said insulating surface, substantially flat electrical leads penetrating and extending into the enclosure and sealed in insulating material, in substantially coplanar arrangement parallel with said insulating surface, and electrical connections between said leads and portions of said body including at least one connection attached to the surface of said body remote from said insulating surface.

The present invention is also a method of manufacturing a hermetically enclosed semiconductor device comprising the steps of securing a semiconductor body to a substantially flat insulating surface on a substrate, sealing a wall portion defining an enclosed area to said substrate and sealing substantially flat electrical leads in insulating material, in substantially coplanar arrangement parallel with said insulating surface and partially within said enclosed area, said body being positioned within said enclosed area, making electrical connections between said leads and portions of said body including the step of attaching a connection to the surface of said body remote from said insulating surface, and securing a cover portion to said wall portion for enclosing the device.

The present invention is also a method of manufacturing a hermetically enclosed semiconductor device comprising the steps of securing a semiconductor body to a substantially flat insulating surface on a substrate with a cement having a temperature coefficient of expansion compatible with those of said insulating surface and said body, thereafter performing process steps on said semiconductor body and completing said hermetically enclosed semiconductor device with said substrate as an external wall of the enclosure.

The method of the present invention therefore lessens or eliminates the problems incident to handling the semiconductive wafers by attaching each semiconductive wafer to an insulating surface on a substrate wafer which is preferably of ceramic material and is preferably sufficiently thick to resist breakage due to normal handling and treating. The semiconductive wafer should be affixed to the insulating surface as early in the processing as is possible and preferably immediately after the semiconductive wafer has been cut to size. The cement employed to bind the semiconductive wafer to the insulating wafer must necessarily be subjected to all of the treatments to which the semiconductive wafer is subjected during the fabrication of the circuit or component therefrom and therefore must meet very severe requirements. The cement used, therefore, is preferably able to withstand the etching solutions normally employed to etch the surface of the semiconductive wafer to the desired configurations and it is preferably also able to withstand treatment temperatures of up to 400°C which could be encountered in normal present day usage. One cement suitable as regards its coefficient of thermal expansion, to semiconductive and insulating wafers used in carrying out the present invention, and which has been found to meet these preferences and thus to be satisfactory in the practice of the present invention, is manufactured by Corning Glass Works under the name Pyroceram Cement No. 95. Pyroceram Cement No. 95 is a low temperature thermal setting cement containing finely powdered glass of a special composition which composition is unknown to us. Nevertheless, many other commercially available sealing compounds are suitable for use as the cements referred to herein.

The method contemplated by the invention according to a preferred embodiment, involves cutting a semiconductive wafer into small wafers and mounting these wafers on a relatively strong ceramic wafer as soon as possible in the manufacturing process with a cement that is insensitive to the treatments to which the semiconductive wafer must be subjected during the fabrication of circuits or components therefrom. By this method a fabrication technique is provided for readily handling very thin semiconductive wafers during etching and forming of contacts and junctions thereon.

After the operations are carried out on the semiconductive wafer to change its physical shape and the electrical properties of predetermined regions thereof, a housing is fastened to the insulating wafer so as hermetically to seal the semiconductive wafer within the housing. The insulating wafer is employed as one side of an enclosure disposed about the semiconductive wafer and the insulating wafer must therefore be sufficiently large to accommodate the other elements of the hermetically sealed housing. If a ceramic wafer is employed as the insulating wafer, the material for cementing the semiconductive wafer to the ceramic substratum must be capable of maintaining a hermetic seal and the aforementioned cement of Corning has been found to be suitable for this purpose.

Where it is desired to apply external ohmic contacts to the semiconductive body, metallic tabs, silver paint or other suitable conductive material may be applied initially to the insulating wafer and the semiconductive wafer may be positioned so as to overlie portions of a conductive strip or conductive strips on the insulating wafer so as to form an electric contact therewith.

In such an arrangement, care must be taken to avoid cement being applied to that area of the semiconductive wafer which is to make electric contact with the conductive elements on the insulating wafer. Further, the conductive material may be applied to the insulating wafer so that it does not contact the semiconductive wafer and a lead or leads may be connected from such conductive strips to various portions of the semiconductive wafer so as to form other contacts therewith. If the insulating wafer is to be employed as a means for making connections to the semiconductive wafer, the insulating wafer would be made substantially larger than the semiconductive wafer so that external leads may be readily connected to the conductive strips applied to the insulating wafer external of the hermetically sealed housing.

Accordingly, in one embodiment of the present invention, a ceramic wafer is initially provided with conductive strips, insulated from one another, which strips constitute all of the required external leads to the circuit. Thereafter, the semiconductive wafer is cemented upon the ceramic wafer as described above so as directly to contact predetermined numbers of the conductive coatings on the ceramic and after treatment of the semiconductor wafer as described above, leads are connected between various predetermined locations on the upper surface of the semiconductive wafer and other of the conductive coatings or metallic strips on the ceramic substrate. Thereafter, a ring of non-conductive ceramic having a height greater than the semiconductive wafer is disposed thereabout and sealed to the ceramic wafer by an insulating cement. The upper surface of this non-conductive ring may be metallized so that a metal plate may be suitably soldered or welded to the upper surface of the ring so as to complete an enclosure about the semiconductive wafer.

In a variation of the aforesaid sealing method, the ring may be formed of metal having a glaze formed about the lower edges thereof by heating a powdered glass in contact therewith and this glaze is sealed, by heating, to a glaze coating of the same size and general configuration as the ring applied to the ceramic substratum. Thereafter a metal plate may be secured to the other side of the metal ring to complete an enclosure.

A hermetically sealed enclosure formed in this way can be provided in less space than is possible by prior art techniques of obtaining hermetic sealed devices. An example of the outline dimensions of a hermetically sealed device such as shown in Figures 1-3 made by a similar process would be a square base of .100" x .100" and a thickness of .020". Even though a device is formed with such minute dimensions, the end product is remarkably rugged and durable in use and these characteristics may be attributed in part to the use of a cemented construction in which the fragile leads extend from between a semiconductor and a ceramic base and through a glaze so that they are reinforced several fold adjacent their point of electrical contact.

Embodiments of the present invention will now be described by way of example, with reference to the accompanying drawings, wherein:

Fig. 1 is a top view of a semiconductor element mounted on a ceramic substrate having conductive leads formed thereon;

Fig. 2 is a cross sectional view in elevation of a structure, incorporating that shown in Fig. 1, in which the ceramic substratum is employed as one element of a hermetically sealed casing or housing disposed about a semiconductor element;

Fig. 3 is a cross sectional view in elevation of a modification of the structure illustrated in Fig. 2;

Fig. 4 is a schematic circuit diagram of a semiconductor network which may be fabricated and packaged in accordance with the present invention;

Fig. 5 is a plan view of the semiconductor network embodying the circuit diagrammed in Fig. 4 and illustrating an embodiment of this invention at one point during its fabrication; and

Fig. 6 is a cross sectional view taken along lines 6-6 of the network shown in Fig. 5.

Referring now specifically to Fig. 1 of the accompanying drawings there is shown an insulating substrate or wafer, preferably a ceramic wafer, to which a small rectangular wafer of semiconductive material 2 is secured by means of a suitable cement as previously described. The wafer 2 may be mounted on the wafer 1 immediately after cutting to desired dimensions and is retained on the wafer 1 throughout all further fabricating operations thereupon.

The fabrication operations which are performed upon the semiconductive wafer may include etching, heating and vapour deposition and other techniques used in the formation of junctions and contacts thereon.

As shown, the wafer 1 has formed on the surface thereof contacting the wafer 2, a plurality of conductive leads or strips indicated by the reference numerals 3, 4, 6 and 7. As illustrated in Fig. 1, the metallized conductors 3, 4 and 6 extend under the wafer 2 so that when the wafer is cemented to the wafer 1 and attached to the leads by solder or conductive cement 5, ohmic contact is established between the wafer 2 and the conductors 3, 4 and 6. The conductor 7, as is readily apparent from Fig. 1, does not extend under the wafer 2 and is employed to make contact via a lead 9 with a junction 8 formed

on the upper surface of the wafer 2. The junction 8 forms a junction diode and the connections to the elements of the diode are established via the conductors 4 and 7.

The specific circuit illustrated in Fig. 1 provides a resistor between the conductors 3 and 6, the resistor constituting the semiconductive material subsisting between those conductors and further a junction diode which subsists between the conductor 4, a center tap to the resistor, and conductor 7. The dispositions of the leads 3, 4, 6, 7 with reference to the wafer 2 are not critical and they may or may not extend beneath the wafer.

Referring now to Fig. 2 of the accompanying drawing there is illustrated a further extension of the apparatus illustrated in Fig. 1. A hermetically sealed casing or housing is formed about the semiconductive wafer 2 and the wafer 1 is employed as one of the elements of the hermetically sealed casing or housing. More specifically, there is provided a metal ring 11 having formed about the bottom and the lower portions of the sides thereof a non-conductive glaze 12. The wafer 1 is provided with a ring of low melting point non-conductive glaze 13 having internal and external diameters which are slightly less and greater respectively, than the internal and external diameters of the ring 11. The ring 11 is positioned on the wafer 1 such that the glaze 12 contacts the glaze 13 formed on the wafer and the structure is heated until the glaze 13 is sufficiently soft to form a bond with the glaze 12. Since the attachment of the glaze 12 to the metal ring 11 is performed remote from the semiconductor 2 this operation may take place at a higher temperature than that required to bond the two glazes 12 and 13 together. In actual practice, the glaze 12 and glaze 13 may be of different powdered glass materials so that the coefficient of heat expansion of each may more nearly correspond to that of the material to which it is directly bonded prior to its being fused to the other glaze. In an alternative embodiment the glaze 13 may be replaced by the aforementioned Corning Pyroceram cement and thereby positively eliminate any potential heat effect on the semiconductor wafer 2 during the bonding procedure. In employing both glazes 12 and 13, the heat effect may be minimized by careful control of the bonding temperature and its duration. Thereafter a metal plate 14 may be soldered or welded to the upper surface of the ring 11 to complete the sealing operation. Obviously, the entire operation preferably takes place in a dry inert atmosphere or in an evacuated chamber, so that any moisture is eliminated from the space within the hermetically sealed casing or housing.

As may be seen from Fig. 2, the ring of glaze 13 is applied to the substrate 1 after the conductive contacts 4 and 7 are in place on the substrate. These contacts may be conductive paint or metallic tabs in which instance the glaze 13 functions to hold the tabs in place on the substrate 1.

It is seen from the above that the wafer 1 serves three distinct functions in the methods described in that it serves as a support for the wafer 2 during its fabrication into the desired physical and electrical configuration, it constitutes a support for the external conductors employed to make various connections to the finished semiconductive structure and further serves as one element of a casing hermetically sealed about the semiconductive wafer or element 2.

Referring now specifically to Fig. 3 of the accompanying drawing, there is illustrated another embodiment of the hermetically sealed casing or housing that may be provided about the semiconductive element 2, which casing or housing also employs the wafer 1 as one of the elements thereof. In this modification of the invention a ring 16 of ceramic, non-conductive material is directly bonded to the wafer 1 through a glaze 13 and the upper surface of the ring is provided with a metallized layer 17. Thereafter, a metal plate 14 may be welded or soldered or otherwise suitably secured to the metallized surface 17 to complete the hermetically sealed casing about the semiconductive element 2.

Referring now specifically to Fig. 4, there is illustrated a multivibrator circuit which is also illustrated in Fig. 7 of the aforesaid copending application. The operation and construction of the circuit illustrated in Fig. 4 will not be discussed except to the extent required to illustrate the present invention. The multivibrator circuit is provided with two transistors T1 and T2 and various external connections to the circuit. An external ground terminal 18 is connected to emitter electrodes 19 and 21 of the transistors T1 and T2, respectively, and an external terminal 22, adapted to be connected to a three volt source, is connected via resistors 23 and 24, to base electrodes 26 and 27 of the transistors T1 and T2, respectively. The base electrode 26 of the transistor T1 is further connected to an input terminal 28 for the transistor T1 and the base 27 is connected to an input terminal 29 for the transistor T2. The transistor T1 is provided with a collector electrode 31 connected to an output terminal 32 of the transistor T1 and the transistor T2 is provided with a collector electrode 33 connected to an output terminal 34 of the transistor T2. The collector electrode 31 of transistor T1 is further connected through a resistor 36 to terminal 37 connected to a negative four volt supply and the collector electrode 33 of the transistor T2 is connected through a resistor 38 to the terminal 37.

Referring now specifically to Figs. 5 and 6 of the accompanying drawing, there is illustrated a semiconductive wafer 39 having formed thereon all the elements illustrated in Fig. 4 of the accompanying drawings. A wafer similar to the wafer 39 is also illustrated in the aforesaid copending application and the wafer 39 may alternatively conform in every detail and respect to the structure described therein. Thus the semiconductor wafer 39 may be of silicon, germanium or an intermetallic alloy. The semiconductor wafer 39 is mounted on a thin metal lead sheet 40 having conductive strips formed therein. Sheet 40 may be formed by etching a very thin sheet of material which has a coefficient of expansion similar to that of silicon, as for example, an alloy of cobalt, nickel and iron known in the trade as KOVAR (Registered Trade Mark). More particularly, the sheet 40 is provided with strips that correspond to the terminals 18, 22, 28, 29, 32, 34 and 37 as illustrated in Fig. 4, and these strips are designated by the function which they serve in the diagram of Fig. 4. More specifically, the strip labeled input T2 corresponds with the terminal 29 of Fig. 4 also designated input T2. The other strips of Fig. 5 serve the corresponding functions as indicated by the references applied thereto. It will be noted that all of the input strips except that labeled "ground" extend under the semiconductive wafer 39 and form contacts therewith, by virtue of the fact that semiconductor wafer 39 is mechanically positioned and subsequently alloyed on top of the strips. A ceramic, glass or other insulating material substrate or wafer 41 of external dimensions substantially equivalent to those of ring 52 is then affixed, as by cement 10, to the back side of the lead sheet 40 and semiconductor wafer 39 to provide reinforcement for this very thin lead sheet and the semiconductor element attached thereto during subsequent fabrication operations as well as during its functional use. Further, the semiconductive wafer 39 is provided with conductive metallized layers 42 and 43 formed by a process of vapour deposition at opposite ends of the semiconductor wafer on the upper surface thereof remote from the sheet 40. The layer 42 is thermally bonded to lead wire 44 and connected via the lead 44 to the base electrode 27 of the transistor T2 and is further connected *via* a lead 46 to the strip designated INP T2, i.e. to the input of T2. The conductive layer 43 is connected *via* a lead 47 to the base electrode 26 of the transistor T1 and further connected *via* a lead 48 to the strip on the lead sheet 40 designated INP T1, i.e. to the input of T1. The emitter electrodes of the transistors T1 and T2 are connected together by a wire lead 49 and are connected via a lead 51 to the strip designated ground. It will be noted that all of the wire leads which are connected to the strips on the sheet 40 lie within a ring 52 which corresponds with the rings 11 and 16 of Figures 2 and 3, respectively. The ring 52 may be ceramic or metal and in either event is sealed to the sheet 40 and the substrate and completely surrounds the semiconductor wafer 39 and the connections thereto. Once the ring 52 has been appropriately secured to the sheet 40 a metal plate similar to plate 14 may be applied thereover and the sealing operation completed.

It will be noted that the sheet 40 is provided with index holes designated by the reference numerals 53 and 54. The holes 53 and 54 are indexing points which may also be in the form of indentations in the sheet 40 and serve to index the sheet and the semiconductor wafer in all of the machinery and other apparatus into which the sheet 40, the substrate 41, and the semiconductor wafer later to form the wafer 39 may be inserted during various fabrication operations. These operations relate to treatment of an original semiconductor wafer to provide the finished wafer 39 by etching of the semiconductive wafer, the formations of junctions and different conductivity regions therein, the formation of a slot 56 therein to isolate certain of the functional areas, the formation of conductive strips 42 and 43 thereon and the attachment of the various leads thereto. The indexing points 53 and 54 also serve to hold the sheet 40 during the application of the semiconductive wafer thereto, the placement of these wafers being critical since accurate alignment between this wafer and the conductive strips on the sheet 40 is essential so as to obtain proper resistance values between various points.

After the semiconductive wafer 39 has been hermetically sealed within its container the sheet 40 may be trimmed along the dashed lines 57 and 58 to form a final assembly in which each of the conductive strips of the sheet 40 are electrically isolated from one another and in which a sufficient area of the strip extends externally of the ring 52 to provide for ready connection of external leads to the conductive strips or insertion of the wafer into printed circuit connectors.

It is apparent from the previous description of the present invention that a method and apparatus for assembly of semiconductive structures is provided in which a relatively small semiconductor wafer may be attached to a ceramic substratum for purposes of supporting the semiconductor wafer during mechanical operations thereon and in which the ceramic substratum thereafter serves a useful purpose in the further fabrication of semiconductor networks and in the final form and structure of such networks.

While several embodiments of this inven-

tion have been described and illustrated, it will be clear that variations of the details of construction which are specifically illustrated and described may be resorted to without departing from the scope of the invention as defined in the appended claims.

WHAT WE CLAIM IS:

1. A hermetically enclosed semiconductor device including a substrate with a substantially flat insulating surface and forming part of an enclosure, a semiconductor body within said enclosure and secured to said insulating surface, substantially flat electrical leads penetrating and extending into the enclosure and sealed, in insulating material, in substantially coplanar arrangement parallel with said insulating surface, and electrical connections between said leads and portions of said body including at least one connection attached to the surface of said body remote from said insulating surface.

2. A semiconductor device according to claim 1, wherein said leads are on said insulating surface.

3. A hermetically enclosed semiconductor device according to either preceding claim, wherein said enclosure includes a wall portion attached to said substrate and an electrically conductive cover portion secured to said wall portion.

4. A hermetically enclosed semiconductor device according to claim 3, wherein said wall portion is electrically conductive.

5. A hermetically enclosed semiconductor device according to any preceding claim, wherein said semiconductor body comprises a semiconductor network, and said electrical connections include a plurality of connections attached to said surface remote from said insulating surface.

6. A hermetically enclosed semiconductor device according to any preceding claim, wherein selected ones of said electrical leads extend between said body and said insulating surface.

7. A hermetically enclosed semiconductor device according to any preceding claim, wherein a cement secures said body to said insulating surface, and said cement, said insulating surface and said body have mutually-compatible temperature coefficients of expansion.

8. A method of manufacturing a hermetically enclosed semiconductor device comprising the steps of securing a semiconductor body to a substantially flat insulating surface on a substrate, sealing a wall portion defining an enclosed area to said substrate and sealing substantially flat electrical leads in insulating material, in substantially coplanar arrangement parallel with said insulating surface and partially within said enclosed area, said body being positioned within said enclosed area, making electrical connections between said leads and portions of said body including the step of attaching a connection to the surface of said body remote from said insulating surface, and securing a cover portion to said wall portion for enclosing the device.

9. A method of manufacturing a hermetically enclosed semiconductor device according to claim 8, including the step of forming said substantially flat electrical leads by shaping a conductive sheet to form integral strips therein.

10. A method of manufacturing a hermetically enclosed semiconductor device according to claim 9, including the step of removing the part of said sheet joining said integral strips after said step of sealing said substantially flat leads.

11. A method of manufacturing a hermetically enclosed semiconductor device comprising the steps of securing a semiconductor body to a substantially flat insulating surface on a substrate with a cement having a temperature coefficient of expansion compatible with those of said insulating surface and said body, thereafter performing process steps on said semiconductor body and completing said hermetically enclosed semiconductor device with said substrate as an external wall of the enclosure.

12. A method of manufacturing a hermetically enclosed semiconductor device according to claim 11, including the steps of forming substantially flat electrical leads in substantially coplanar arrangement, sealing said leads in insulating material parallel with said insulating surface and partially within the enclosure, and wherein said process steps performed on said semiconductor body include making electrical connection between some of said electrical leads and portions of said semiconductor body by attaching connections to the surface of said body remote from said insulating surface.

13. A method of manufacturing a hermetically enclosed semiconductor device according to claim 11 or 12, wherein said process steps performed on said semiconductor body include carrying out operations on the body to change the physical shape and the electrical properties of predetermined regions of said body.

14. A method of manufacturing a hermetically enclosed semiconductor device according to claim 12, wherein said step of forming includes the step of shaping a conductive sheet to form integral strips therein.

15. A method of manufacturing a hermetically enclosed semiconductor device according to claim 14, including the step of separating said integral strips from said conductive sheet after said step of sealing.

16. A hermetically enclosed semiconductor device when produced by the method of any of claims 8 to 15.

17. A method for producing the device

tion have been described and illustrated, it will be clear that variations of the details of construction which are specifically illustrated and described may be resorted to without departing from the scope of the invention as defined in the appended claims.

WHAT WE CLAIM IS:

1. A hermetically enclosed semiconductor device including a substrate with a substantially flat insulating surface and forming part of an enclosure, a semiconductor body within said enclosure and secured to said insulating surface, substantially flat electrical leads penetrating and extending into the enclosure and sealed, in insulating material, in substantially coplanar arrangement parallel with said insulating surface, and electrical connections between said leads and portions of said body including at least one connection attached to the surface of said body remote from said insulating surface.

2. A semiconductor device according to claim 1, wherein said leads are on said insulating surface.

3. A hermetically enclosed semiconductor device according to either preceding claim, wherein said enclosure includes a wall portion attached to said substrate and an electrically conductive cover portion secured to said wall portion.

4. A hermetically enclosed semiconductor device according to claim 3, wherein said wall portion is electrically conductive.

5. A hermetically enclosed semiconductor device according to any preceding claim, wherein said semiconductor body comprises a semiconductor network, and said electrical connections include a plurality of connections attached to said surface remote from said insulating surface.

6. A hermetically enclosed semiconductor device according to any preceding claim, wherein selected ones of said electrical leads extend between said body and said insulating surface.

7. A hermetically enclosed semiconductor device according to any preceding claim, wherein a cement secures said body to said insulating surface, and said cement, said insulating surface and said body have mutually-compatible temperature coefficients of expansion.

8. A method of manufacturing a hermetically enclosed semiconductor device comprising the steps of securing a semiconductor body to a substantially flat insulating surface on a substrate, sealing a wall portion defining an enclosed area to said substrate and sealing substantially flat electrical leads in insulating material, in substantially coplanar arrangement parallel with said insulating surface and partially within said enclosed area, said body being positioned within said enclosed area, making electrical connections between said leads and portions of said body including the step of attaching a connection to the surface of said body remote from said insulating surface, and securing a cover portion to said wall portion for enclosing the device.

9. A method of manufacturing a hermetically enclosed semiconductor device according to claim 8, including the step of forming said substantially flat electrical leads by shaping a conductive sheet to form integral strips therein.

10. A method of manufacturing a hermetically enclosed semiconductor device according to claim 9, including the step of removing the part of said sheet joining said integral strips after said step of sealing said substantially flat leads.

11. A method of manufacturing a hermetically enclosed semiconductor device comprising the steps of securing a semiconductor body to a substantially flat insulating surface on a substrate with a cement having a temperature coefficient of expansion compatible with those of said insulating surface and said body, thereafter performing process steps on said semiconductor body and completing said hermetically enclosed semiconductor device with said substrate as an external wall of the enclosure.

12. A method of manufacturing a hermetically enclosed semiconductor device according to claim 11, including the steps of forming substantially flat electrical leads in substantially coplanar arrangement, sealing said leads in insulating material parallel with said insulating surface and partially within the enclosure, and wherein said process steps performed on said semiconductor body include making electrical connection between some of said electrical leads and portions of said semiconductor body by attaching connections to the surface of said body remote from said insulating surface.

13. A method of manufacturing a hermetically enclosed semiconductor device according to claim 11 or 12, wherein said process steps performed on said semiconductor body include carrying out operations on the body to change the physical shape and the electrical properties of predetermined regions of said body.

14. A method of manufacturing a hermetically enclosed semiconductor device according to claim 12, wherein said step of forming includes the step of shaping a conductive sheet to form integral strips therein.

15. A method of manufacturing a hermetically enclosed semiconductor device according to claim 14, including the step of separating said integral strips from said conductive sheet after said step of sealing.

16. A hermetically enclosed semiconductor device when produced by the method of any of claims 8 to 15.

17. A method for producing the device

of any of claims 1 to 7 substantially as described herein with reference to the accompanying drawings.

18. A hermetically enclosed semiconductor device substantially as described herein with reference to the accompanynig drawings.

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ERRATA

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AMENDMENT NO. 1

Page No. 2, line 3, *after* "with" *insert* "a"

Page No. 4, line 11, *for* "center" *read* "centre"

THE PATENT OFFICE,
28th May, 1965

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