

FIR FILTER APPARATUS FOR PROCESSING OF TIME DIVISION
MULTIPLEXED SIGNALS

ABSTRACT

FIR filter circuitry for processing time division multiplexed sampled signals includes parallel sets of delay elements (D_{SP} , D_{HP}), for delaying respective signals to be filtered, each set having a plurality of taps. Corresponding taps of the
5 respective sets of delay elements are coupled to common weighting (W_{n+i}) and summing structure (Adder). A time division multiplexed signal is coupled to the parallel sets of delay elements, respective sets being exclusively (D_{SP} Clk, D_{HP} Clk)
10 clocked on the occurrence of corresponding signals.

This Sheet Has Been Replaced



FIGURE 8