METHOD OF SEMICONDUCTOR MANUFACTURE

This invention relates generally to methods of making semiconductors. More specifically, the present invention relates to methods applicable when changing the effective position of ("re-routing") bond pads.

After an integrated circuit (IC) has been made, it is necessary to package it in a way that will allow it to be connected to a circuit board. This involves providing input/output terminals so that the semiconductor may communicate with other segments of the electronic/electrical system. This is usually accomplished by providing bond pads on the IC which can have wires attached to them by solder. In order to achieve greater accessibility and flexibility, it is often necessary to change the position of the bond pads already present on an IC.

Presently, such re-routing may be carried out in accordance with the method schematically illustrated in Figure 1 of the accompanying drawings. This method comprises placing a patterned metal layer 1 onto a passive layer 2 on a semiconductor chip 3 such that the metal layer comes into contact with the exposed bond pad 4 (see Figures 1a and 1b). Another layer of passive material 5 is then laid over the metal layer (Figure 1c). A portion of the second layer of passive material 5 is then etched so that a part 6 of the metal layer at a position different to the original bond pad position is exposed (see Figure 1d). This effectively changes the position of the bond pad 4 to a new position.

The problem with this prior method is that the process used for laying the metal layer is an expensive and lengthy process known as physical vapour deposition (PVD). This process involves the spraying of minute metal particles onto the surface of the passive layer until a complete coating of a very thin layer of metal is achieved. This process is also known as "sputtering". The equipment required for this method is very expensive and the process takes a long time to carry out (an average of an hour or so for some machines).

An aim of the present invention is to provide a method for re-routing a bond pad which avoids the need for a sputtering process.

According to a first aspect of the present invention there is provided a

method of re-routing a bond pad of a semiconductor element, said method comprising:

providing a semiconductor element having at least one bond pad on an outer surface thereof;

depositing a layer of dielectric on said semiconductor element so to cover said bond pad;

patterning said dielectric layer to reveal at least part of said bond pad;

depositing a layer of copper on said semiconductor element so that said copper layer is in electrical connection with said bond pad;

applying a patterned layer of photoresist on said copper layer;

etching to remove parts of the copper layer not covered by said photoresist;

applying a passivation layer to said resulting structure;

removing some of said passivation layer to expose part of said copper layer.

Accordingly, the present invention provides a method for re-routing bond pads which avoids the sputtering process altogether. Therefore, the method of the present invention is less expensive and is able to be carried out in a shorter time than conventional methods.

The invention is applicable to all known wafer substrates including those made of gallium arsenide or silicon.

Preferably, the bond pad comprises a layer of nickel or gold deposited on the semiconductor structure.

In order to deposit such nickel or gold layers, it is preferred to use a sodium hypophosphite based bath at a temperature in the range of 70 to 90°C for a duration in the range of 20 to 30 minutes as an electroless plating bath.

The present invention will be further described by way of non-limitative example only, with reference to the accompanying schematic drawings, in which:

Figure 1 illustrates in joint cross-sectional side-on view and plan view a known prior art method of re-routing a bond pad;

Figure 2 illustrates in joint cross-sectional side-on view and plan view a method of re-routing a bond pad according to an embodiment of the present invention;

Figure 3 is a flow diagram showing the dielectric deposition and patterning steps according to the invention; and

Figure 4 is a flow diagram showing the electroless/electrolytic copper plating method according to the invention.

The method of rerouting a bond pad of a semiconductor element in accordance with the present invention will now be described with reference to Figure 2.

In the embodiment, the semiconductor element 20 contains a single bond pad 21 on the right-hand side of the element which is desired to be re-routed to the left-hand side. The invention is not only applicable to elements having a single bond pad but may be applied to multi-pad elements. The exact final configuration of re-routed bond pads is determined by the single lithography step described later.

A typical semiconductor structure is shown in Figure 2a. The bond pad 21 is usually integrally provided in the semiconductor substrate 20 and the substrate 20 is usually completely covered with a layer of passivation 22 (for example; polyimide, BCB, silicon nitride, silicon oxynitride or silicon dioxide), except for small portions where the bond pad 21 is exposed through the passivation layer 22. The invention concerns a particular method for moving the effective position of the bond pad 21 by adding various layers in a predetermined order. Usually, semiconductor wafers are manufactured with the passivation layer 22 already provided. However, occasionally, this is not the case. This is not of concern in the present case because the present invention is applicable to semiconductor wafers provided with or without passivation layer 22. The following description assumes a layer 22 is present, but the invention still works if this is not the case.

The first step involves plating the bond pad 21 with a metal 23 to raise the effective level of the bond pad to be the same as, or slightly higher than, the top surface of the layer of passivation 22. This creates a new bond pad 23. This metal plating step is preferably achieved using an electroless method and nickel or gold are preferably used for this purpose. An electroless nickel plating method will now be described. It firstly comprises cleaning the surface of the bond pad in an alkaline solution to remove any oxide.

Then, a layer of organic coating is applied to the back side of the semiconductor wafer 20 to protect it (not shown). This leaves all of the surfaces of the wafer isolated except for the bond pad surface.

Next, the entire structure is immersed in a fluid which activates the bond pad and makes it receptive to the next stage, which is the nickel plating stage. This immersion step is called "zincation". For this zincation step, the fluid used is based on a zinc salt and is preferably between 30 and 70°C. The zincation step usually takes around 10 to 15 minutes. The wafer may be wholly or partially immersed; it is only necessary that the bond pad itself receives the zincation treatment.

After this preparatory step, the nickel plating is deposited using the electroless method. As the name implies, no electric current is required to be fed through the bath in which the wafer is submerged in for nickel plating to occur. The method comprises partially or wholly submerging the substrate in a nickel plating bath which deposits a layer of nickel plating on the bond pad. This depositing occurs because the bond pad 21 has been made receptive to receive the nickel by the zincation step.

The amount of nickel deposited is dependent upon the duration and temperature at which the wafer is submerged in the bath. The nickel is allowed to build up in height so that the top surface of the nickel plating 23 is the same as or higher than the top surface of the layer of passivation 22 on the semiconductor 20. The nickel plated bond pad is thus flush with the passivation layer 22 in order to receive a dielectric layer 24 (see Figure 2b).

The nickel plating bath comprises a nickel based salt fluid. For this step, the temperature is preferably maintained between 70 and 90°C and a duration of between about 10 to 15 minutes is generally sufficient to produce a nickel layer of appropriate thickness.

After the electroless nickel plating step, a layer of dielectric 24 is provided over the entire top surface of the structure (see Figure 2c). This is achieved by coating the top surface of the structure with the dielectric material and then baking the structure to harden it. This dielectric layer has "plateable" characteristics in that it allows one to next apply a copper layer thereon (via an electroless method) without

the need for plasma desmearing. Plasma desmearing is slightly disadvantageous because it can cause a potential weak point as a result of rapid material removal.

A patterning process is then carried out using a mask 25 which allows light to pass through it only in the area not occupied by the bond pad 21. This provides a bond pad-shaped hole in the dielectric 24 so that the nickel plating 23 is exposed to the outside of the structure. This procedure is shown schematically in Figure 2d. The dielectric is patterned using ultraviolet radiation and after this is cured. A flow chart showing the process for dielectric deposition and patterning is shown in Figure 3 and the process will now be described in more detail. As will be seen from the flow chart, a coating of the plateable dielectric of 15 - 50 microns is first applied to the structure (Figure 2c). Either a spin coater or a screen printer can be used for this purpose which can be carried out at room temperature (23° to 30°C).

Next, a softbake/tack dry step is used to remove the residual solvent prior to exposing a pattern on the dielectric. This is carried out using a hot plate or dust-free convection oven at a typical temperature of 68° to 74°C for about 30 to 45 minutes.

The exposure process shown in Figure 2d is carried out using an exposure machine (typical power 3 to 5 kilowatts) which provides ultraviolet radiation in a typical range of 400 to 450 millijoules per square centimetre at room temperature.

A developing process is then carried out which allows dissolution of the unexposed areas and preservation of the exposed areas of dielectric. This can be achieved in a tank comprising a heater which heats the structure to 36° to 40°C. This process takes approximately 2 to 3 minutes and uses a concentrate of sodium carbonate in the range of 0.8 to 1.2%.

After this step, a post-curing step is carried out to initiate further polymerization and cross-linking of the dielectric in preparation for the subsequent baking process. An ultraviolet pump machine providing an ultraviolet radiation dosage of 3 joules per square centimetre is provided for this step.

Finally, a baking step is carried out to complete the cross-linking and polymerization of the dielectric so that the chemical and physical performance of the dielectric is optimized. This is achieved in a dust-free convection oven having a temperature of 135°C. A typical processing time is 1 hour.

The next step involves laying a complete layer of copper 26 over the entire top surface of the structure. This layer of copper 26 is deposited on the top surface using the two-stage process of a combined electroless/electrolytic plating method. This method comprises firstly using an electroless copper plating step to achieve a copper plating thickness of between 0.5 and 1 micron and subsequently using an electrolytic copper plating step to achieve a plating thickness of between 5 to 10 microns. The electroless method is slightly slower than the electrolytic method but is required because one cannot use an electrolytic method unless there is already a thin copper layer to start with. The electroless method provides this thin starting layer after which the faster electrolytic method is used. A flow chart showing this electroless/electrolytic copper plating method is shown in Figure 4.

The first stage of this process is to further prepare the nickel surface 23 after the patterning step. This step is referred to as "Conditioner I" in the flow chart of Figure 4. It involves immersing the top of the substrate in a carefully balanced mixture of acid salts, activators and surface active agents to prepare the nickel surface. A temperature of between 50 to 60°C and an immersion time of 5 minutes is used. The solution in the bath is stirred using a magnetic stirrer.

Next, the substrate is rinsed in de-ionised (DI) water at a room temperature of about 23-30°C. A second conditioning step (referred to as "Conditioner II" in Figure 4) is then carried out to prepare the dielectric surface 24. This is a two-stage process for cleaning and conditioning the dielectric surface using an inorganic mixture..

Next, a further water rinsing step is carried out before an activator pre-dip step. The activator pre-dip stage is used to prepare the surface for uniform adsorption of the activator. This stage lasts about a minute and is carried out at room temperature. It involves submerging the substrate in a chloride solution in a tank.

The next stage is referred to as the "Activator" stage in the flow diagram of Figure 4. This involves providing a small, high charge-density palladium-tin chloride colloid layer which promotes a uniform and well adhered electroless copper deposit. The amount of Palladium is preferably 1.2-1.4% by volume of water. This is carried out at room temperature and lasts about 5 minutes.

Next, the substrate is rinsed with water at room temperature before being

bathed in an accelerator. The accelerator is an alkaline based solution comprising two components. It optimises the catalytic activity of the activator. A pH of between 8 and 9 is used and the step lasts about 2 ½ minutes.

Next, the electroless copper plating step is carried out after a water rinse. This step is similar to the nickel plating step in that it involves submerging the structure in a copper solution bath. A plating thickness of between 0.5 and 1 micron is achievable in 30 to 40 minutes of processing. The solution comprises copper in the amount of approximately 6.5 to 8.5 grams per litre. The solution also comprises 35 to 45 grams per litre of reducer. The reducer serves to reduce copper ions into metallic copper and comprises a hypophosphite based chemical. The pH is maintained at between 8.2 and 8.6 and a temperature of between 71 to 80°C is required. The solution is kept moving using a magnetic stirrer and air agitation is necessary.

Next, an electrolytic method of plating copper is used. The electroless copper plated substrate is firstly rinsed in water before being immersed in an acid copper pre-dip for between 30 and 40 seconds. This pre-dip stage prepares the surface for uniform electrolytic plating. The solution comprises a low acid solution at room temperature.

The electrolytic copper plating stage is then carried out. This plating process makes use of an electric current to transfer the anions and cations to the relevant species causing reduction of the metal ions and deposition of metal onto the cathode. A cup plating system is used with a plating current density of between 1.8 and 2.8 amperes per square metre. The copper plating solution comprises 70 to 80 grams per litre of copper sulphate, 180 to 210 grams per litre of sulphuric acid and a chloride composition of 50 to 70 parts per million. This process lasts for about 5 minutes to 15 minutes to obtain a plating thickness of between 5 and 10 microns.

The substrate is then subjected to a water rinse, an anti-tarnishing step, a further water rinse and a drying step. Each of these steps are carried out at room temperature, and the anti-tarnishing step takes about 1 minute. The anti-tarnishing step comprises laying a thin coating over the copper to prevent oxidation thereof. For the drying step, a nitrogen purge is desirable which involves drying in an

atmosphere of only nitrogen gas.

Referring back to Figure 2, the copper plated semiconductor is shown in Figure 2f.

Next, a layer of photoresist 27 is applied to the surface of the copper plate in the conventional manner, the photoresist pattern corresponding to the desired re-route of the bond pad (see Figure 2g). A copper etching step is then carried out to remove the copper not protected by the layer of photoresist. This leaves a copper re-route 28 electrically connected with the bond pad 21 on the surface of the passivation 24 on the semiconductor 20. This is shown in Figure 2h.

A further layer of passivation 29 is then applied to the entire surface of the structure to completely cover the copper re-route 28 as shown in Figure 2i. This layer is preferably 15 to 25 microns in thickness. A lithography step is then carried out to expose one end of the copper reroute through the layer of passivation as shown in Figure 2j. The exposed part of the re-route 30 is then optionally plated with nickel or gold 31, preferably using the electroless process described earlier. This is shown in Figure 2k.

Finally, some solder 32 is placed on the nickel/gold plated part 31 and is heated so that it adheres to the structure. This heating (termed "reflow") also causes the solder 31 to change to a more appropriate shape for connections to be made. This is shown in Figures 2l and 2m.

The result of the above process is that the bond pad has been effectively moved from the right of the semiconductor to the left side of the semiconductor.

The method according to the present invention is desirable because it completely avoids the sputtering process conventionally used. The invention instead relies on very low cost chemical based processes which allow very easy control by varying the time and conditions. For example, the plating thicknesses can easily be controlled by adjusting the amount of time the structure is immersed in the bath. The process of the present invention is also desirable in that it allows a re-routing processing plant to be established without expensive machinery and thus at low cost when compared to methods involving a sputtering process.

Although the total number of steps of the method of the present invention is

more than in a conventional prior art process involving a sputtering method, the advantages obtained in terms of time, expense and throughput outweigh the additional complexity.

The above methods are suitable for all semiconductor wafers known in the industry, including GaAs and silicon wafers.

* C L M S *

CLAIMS

1. A method of re-routing a bond pad of a semiconductor element, said method comprising:

providing a semiconductor element having at least one bond pad on an outer surface thereof;

depositing a layer of dielectric on said semiconductor element so to cover said bond pad;

patterning said dielectric layer to reveal at least part of said bond pad;

depositing a layer of copper on said semiconductor element so that said copper layer is in electrical connection with said bond pad;

applying a patterned layer of photoresist on said copper layer;

etching to remove parts of the copper layer not covered by said photoresist;

applying a passivation layer to said resulting structure;

removing some of said passivation layer to expose part of said copper layer.

2. A method according to claim 1, wherein said bond pad comprises a layer of metal on said semiconductor structure.

3. A method according to any one of the preceding claims wherein said step of patterning said dielectric layer comprises a coating step, a first baking step, an exposure step, a developing step, a curing step and a second baking step.

4. A method according to claim 3, wherein said coating step comprises coating said semiconductor element with dielectric material having a thickness from 15 to 50 microns.

5. A method according to claim 3 or 4, wherein said first baking step comprises heating the entire structure for 30-45 minutes at a temperature of from 68 - 74°C.

6. A method according to claim 3, 4 or 5, wherein said exposure step comprises exposing to ultraviolet light said dielectric layer apart from an area adjacent to said bond paid.

7. A method according to claim 6, wherein said ultraviolet light has an energy density of 400 - 450 mJ/cm^2.

8. A method according to any one of claims 3 to 7, wherein said developing step comprises immersing in a concentrate of sodium carbonate at from 36 - 40°C for 2 - 3 minutes.

9. A method according to any one of claims 3 to 8, wherein said curing step comprises exposing said dielectric layer to ultraviolet radiation having an energy density of about 3J/cm^2.

10. Aa method according to any one of claims 3 to 9, wherein said second baking step comprises heating the entire structure for about 60 minutes at a temperature of about 135°C.

11. An integrated circuit board comprising at least one semiconductor chip produced using a method according to any preceding claim.

12. A method of making a semiconductor chip comprising the method of any one of claims 1 to 10.

13. A method of re-routing a bond pad substantially as hereinbefore described with reference to Figures 2, 3 and 4 of the accompanying drawings.