What is claimed is:

1. A Fin field effect transistor (FinFET) comprising:

a substrate comprising a top surface;

a first fin and a second fin extending above the substrate top surface, wherein the first fin has a top surface and sidewalls and the second fin has a top surface and sidewalls;

an insulation layer between the first and second fins extending part way up the fins from the substrate top surface;

a first gate dielectric covering the top surface and sidewalls of the first fin having a first thickness t1 and a second gate dielectric covering the top surface and sidewalls of the second fin having a second thickness t2 less than the first thickness; and

a conductive gate strip traversing over both the first gate dielectric and the second gate dielectric.

2. The FinFET of claim 1, wherein a portion of the first fin extending above the insulation layer is thinner than a portion of the second fin extending above the insulation layer.

3. The FinFET of claim 1, wherein a ratio of a width of a portion of the first fin extending above the insulation layer to a width of a portion of the second fin extending above the insulation layer is from 0 to 0.95.

4. The FinFET of claim 1, wherein the top surface of the first fin is lower than the top surface of the second fin.

5. The FinFET of claim 1, wherein a ratio of a height of the first fin above the insulation layer to a height of the second fin above the insulation layer is from 0 to 0.95.

6. The FinFET of claim 1, wherein a top surface of the insulation layer is lower than the top surface of the first fin.

7. The FinFET of claim 1, wherein a ratio of the first thickness to the second thickness is from 1.05 to 2.

8. The FinFET of claim 1, wherein the conductive gate strip comprises an N-work function metal, wherein the transistor is an n-type FinFET.

9. The FinFET of claim 8, wherein the N-work-function metal comprises a metal selected from a group consisting of Ti, Ag, Al, TiAl, TiAlN, TaC, TaCN, TaSiN, Mn, and Zr.

10. The FinFET of claim 9, wherein the FinFET is operated while turning on the second fin and not turning on the first fin.

11. The FinFET of claim 1, wherein the conductive gate strip comprises a P-work function metal, wherein the transistor is a p-type FinFET.

12. The FinFET of claim 11, wherein the P-work-function metal comprises a metal selected from a group consisting of TiN, WN, TaN, and Ru.

13. A Fin field effect transistor (FinFET) comprising:

a substrate comprising a top surface;

a first fin and a second fin extending above the substrate top surface, wherein the first fin has a top surface and the second fin has a top surface and sidewalls;

an insulation layer between the first and second fins extending part way up the fins from the substrate top surface, wherein a top surface of the insulation layer is substantially coplanar with the top surface of the first fin;

a first gate dielectric covering the top surface of the first fin having a first thickness and a second gate dielectric covering the top surface and sidewalls of the second fin having a second thickness less than the first thickness; and

a conductive gate strip traversing over both the first gate dielectric and the second gate dielectric.

14. The FinFET of claim 1, wherein the top surface of the first fin is lower than the top surface of the second fin.

15. A method of fabricating a Fin field effect transistor (FinFET) comprising:

providing a substrate having a first fin and a second fin extending above a substrate top surface, wherein the first fin has a top surface and sidewalls and the second fin has a top surface and sidewalls;

forming an insulation layer between the first and second fins extending part way up the fins from the substrate top surface;

forming a photo-sensitive layer over the first and second fins;

patterning the photo-sensitive layer to expose the portion of the first fin above the insulation layer and cover the second fin;

forming a first gate dielectric having a first thickness covering the top surface and sidewalls of the first fin using a plasma doping process;

removing the photo-sensitive layer;

forming a second gate dielectric covering the top surface and sidewalls of the second fin having a second thickness less than the first thickness; and

forming a conductive gate strip traversing over both the first gate dielectric and the second gate dielectric.

16. The method of claim 15, wherein the plasma doping process comprises an oxygen-containing plasma doping process.

17. The method of claim 16, wherein the plasma doping process is performed under a source power of about 260 to 2500W.

18. The method of claim 17, wherein the plasma doping process is performed under a pressure of about 1 mTorr to 50 mTorr.

19. The method of claim 15 further comprising:

annealing the first gate dielectric after the plasma doping process.

20. The method of claim 15 further comprising:

simultaneously annealing the first gate dielectric and the second gate dielectric after forming the second gate dielectric.

CLAIMS

1. A Fin field effect transistor (FinFET) comprising:

a substrate comprising a top surface;

a first fin and a second fin extending above the substrate top surface, wherein the first fin has a top surface and sidewalls and the second fin has a top surface and sidewalls;

an insulation layer between the first and second fins extending part way up the fins from the substrate top surface;

a first gate dielectric covering the top surface and sidewalls of the first fin having a first thickness t1, wherein the first gate dielectric is in direct contact with the first fin;

a second gate dielectric covering the top surface and sidewalls of the second fin having a second thickness t2 less than the first thickness, wherein the second gate dielectric is in direct contact with the second fin; and

a conductive gate strip traversing over both the first gate dielectric and the second gate dielectric.

2. The FinFET of claim 1, wherein a portion of the first fin extending above the insulation layer is thinner than a portion of the second fin extending above the insulation layer.

3. The FinFET of claim 1, wherein a ratio of a width of a portion of the first fin extending above the insulation layer to a width of a portion of the second fin extending above the insulation layer is from 0 to 0.95.

4. The FinFET of claim 1, wherein the top surface of the first fin is lower than the top surface of the second fin.

5. The FinFET of claim 1, wherein a ratio of a height of the first fin above the insulation layer to a height of the second fin above the insulation layer is from 0 to 0.95.

6. The FinFET of claim 1, wherein a top surface of the insulation layer is lower than the top surface of the first fin.

7. The FinFET of claim 1, wherein a ratio of the first thickness to the second thickness is from 1.05 to 2.

8. The FinFET of claim 1, wherein the conductive gate strip comprises an N-work function metal, wherein the transistor is an n-type FinFET.

9. The FinFET of claim 8, wherein the N-work-function metal comprises a metal selected from a group consisting of Ti, Ag, Al, TiAl, TiAlN, TaC, TaCN, TaSiN, Mn, and Zr.

10. The FinFET of claim 9, wherein the FinFET is operated while turning on the second fin and not turning on the first fin.

11. The FinFET of claim 1, wherein the conductive gate strip comprises a P-work function metal, wherein the transistor is a p-type FinFET.

12. The FinFET of claim 11, wherein the P-work-function metal comprises a metal selected from a group consisting of TiN, WN, TaN, and Ru.

13. The FinFET of claim 1, wherein the top surface of the first fin is lower than the top surface of the second fin.

14. A Fin field effect transistor (FinFET) comprising:

a substrate comprising a top surface;

a first fin and a second fin extending above the substrate top surface, wherein the first fin has a top surface and the second fin has a top surface and sidewalls;

an insulation layer between the first and second fins extending part way up the fins from the substrate top surface, wherein a top surface of the insulation layer is substantially coplanar with the top surface of the first fin, and the second fin protrudes from the insulation layer;

a first gate dielectric covering the top surface of the first fin having a first thickness;

a second gate dielectric covering the top surface and sidewalls of the second fin having a second thickness less than the first thickness; and

a conductive gate strip traversing over both the first gate dielectric and the second gate dielectric.

15. A Fin field effect transistor (FinFET) comprising:

a substrate comprising a top surface;

a first fin extending above the top surface of the substrate, wherein the first fin has a top surface and sidewalls;

a second fin extending above the top surface of the substrate, wherein the second fin has a top surface and sidewalls;

an insulation layer between the first fin and the second fin, the insulation layer covering a portion of the first fin and a portion of the second fin, wherein a portion of the first fin below a top surface of the insulation layer has a width substantially equal to a width of the second fin, and a portion of the first fin above the top surface of the insulation layer has a width less than the width of the second fin;

a first gate dielectric over the top surface of the first fin, the first gate dielectric having a first thickness over the top surface of the first fin;

a second gate dielectric over the top surface and sidewalls of the second fin, the second gate dielectric having a second thickness less than the first thickness; and

a conductive gate strip traversing over both the first gate dielectric and the second gate dielectric.

16. The FinFET of claim 15, wherein the second gate dielectric is between the first gate dielectric and the conductive gate strip.

17. The FinFET of claim 15, wherein the first gate dielectric covers the sidewalls of the first fin.

18. The FinFET of claim 15, wherein the top surface of the first fin is level with a top surface of the insulation layer.

19. The FinFET of claim 15, wherein a width of the first fin above the insulation layer is less than a width of the second fin above the insulation layer.

20. The FinFET of claim 15, wherein a height of the first fin is less than a height of the second fin.