

ABSTRACT

A video signal processing circuit synthesizes a video signal and a graphic signal on the basis of a display switching control signal, inverts a synthesized signal on the time axis for each of a forward scanning period and a backward scanning period, and output a display signal. A speed modulating signal control circuit inverts the binarized display switching control signal on the time axis for each of the forward scanning period and the backward scanning period, expands the pulse width thereof, and feeds the display switching control signal to a speed modulating signal generating circuit. The speed modulating signal generating circuit subjects a display signal to first-order differentiation, inverts the polarity of a differentiated signal in the backward scanning signal, sets a portion, corresponding to the graphic signal, in the differentiated signal on the basis of the display switching control signal at a zero level, and generates a speed modulating signal.