ELECTROPLATED INTERCONNECTION STRUCTURES ON INTEGRATED CIRCUIT CHIPS

Field of the Invention

This invention relates to interconnection wiring on electronic devices such as on integrated circuit (IC) chips and more particularly to void-free and seamless submicron structures fabricated by Cu electroplating from baths that contain additives conventionally used to produce bright, level, low-stress deposits.

Background of the Invention

AlCu and its related alloys are a preferred alloy for forming interconnections on electronic devices such as integrated circuit chips. The amount of Cu in AlCu is typically in the range from .3 to 4 percent.

Replacement of AlCu by Cu and Cu alloys as a chip interconnection material results in advantages of performance. Performance is improved because the resistivity of Cu and certain copper alloys is less than the resistivity of AlCu; thus narrower lines can be used and higher wiring densities will be realized.

The advantages of Cu metallization have been recognized

by the entire semi-conductor industry. Copper metallization has been the subject of extensive research as documented by two entire issues of the Materials Research Society (MRS) Bulletin, one dedicated to academic research on this subject in MRS Bulletin, Volume XVIII, No. 6 (June 1993) and the other dedicated to industrial research in MRS Bulletin, Volume XIX, No. 8 (August 1994). A 1993 paper by Luther et al., *Planar Copper-Polyimide Back End of the Line Interconnections for ULSI Devices*, in PROC. IEEE VLSI MULTILEVEL INTERCONNECTIONS CONF., Santa Clara, CA, June 8-9, 1993, p. 15, describes the fabrication of Cu chip interconnections with four levels of metallization.

Processes such as Chemical Vapor Deposition (CVD) and electroless plating are popular methods for depositing Cu. Both methods of deposition normally produce at best conformal deposits and inevitably lead to defects (voids or seams) in wiring especially when trenches have a cross section narrower at the top than at the bottom as a result of lithographic or reactive ion etching (RIE) imperfections. Other problems of CVD have been described by Li et al., *Copper-Based Metallization in ULSI Structures - Part II: Is Cu Ahead of its Time as an On-chip Material?*, MRS BULL., XIX, 15 (1994). In electroless plating, while offering the advantage of low cost, the evolution of hydrogen during metal deposition leads to blistering and other defects that are viewed as weaknesses for industry wide implementation.

An electroplating process for depositing copper, silver or gold onto a semiconductor wafer is described in US Patent 5,256,274 ('274), which issued on October 26, 1993, to J. Poris. In Fig. 1A of '274, a copper conductor is shown with a seam in its center with the legend "GOOD" and in Fig. 1B a copper conductor is shown with a void in its center with the legend "BAD." The plating bath contained 12 ounces/gallon of water of $CuSO_4$, $5H_2O$, 10% by volume of concentrated sulfuric acid, 50 parts per millions of chloride ion from hydrochloric acid, and TECHNI-COPPER W additive 0.4 % by volume provided by Technic Inc., P.O. Box 965, Providence, RI 02901. Plating was selectively deposited through an inert mask.

Summary of the Invention

A process is described for fabricating a low cost, highly reliable Cu interconnect structure for wiring in integrated circuit chips with void-free seamless conductors of sub-micron dimensions. The process comprises deposition of an insulating material on a wafer, lithographically defining and forming sub-micron trenches or holes in the insulating material into which the conductor will be deposited to ultimately form lines or vias, depositing a thin conductive layer serving as a seed layer or plating base, depositing the conductor by electroplating from a bath containing additives and planarizing or chemical-mechanical polishing the resulting structure to accomplish electrical isolation of individual

lines and/or vias.

The invention further provides a process for fabricating an interconnect structure on an electronic device comprising the steps of forming a seed layer on a substrate having insulating regions and conductive regions, forming a patterned resist layer on the seed layer, electroplating conductor material on the seed layer not covered by the patterned resist from a bath containing additives, and removing the patterned resist.

The invention further provides a process for fabricating an interconnect structure on an electronic device with void-free seamless conductors comprising the steps of forming an insulating material on a substrate, lithographically defining and forming lines and/or vias in which interconnection conductor material will be deposited, forming a conductive layer serving as a plating base, forming a patterned resist layer on the plating base, depositing the conductor material by electroplating from a bath containing additives, and removing the resist.

The invention further provides a process for fabricating an interconnect structure on an electronic device comprising the steps of forming a seed layer on a substrate having insulating regions and conductive regions, forming a blanket layer of conductor material on the seed layer from a bath

containing additives, forming a patterned resist layer on the blanket layer, removing the conductor material where not covered by the patterned resist, and removing the patterned resist. The invention further provides a conductor for use in interconnections on an electronic device comprising Cu including small amounts of a material in the Cu selected from the group consisting of C (less than 2 weight percent), O (less than 1 weight percent), N (less than 1 weight percent), S (less than 1 weight percent), and Cl (less than 1 weight percent) formed by electroplating from a bath containing additives.

The interconnection material may be Cu electroplated from baths that contain additives conventionally used to produce bright, level, low-stress deposits. The rate of Cu electroplating from such baths is higher deep within cavities than elsewhere. This plating process thus exhibits unique superfilling properties and results in void-free seamless deposits that cannot be obtained by any other method. Interconnection structures made by Cu electroplated in this manner, are highly electromigration-resistant with an activation energy for electromigration equal to or greater than 1.0 eV. The conductor is composed substantially of Cu and small amounts of atoms and/or molecular fragments of C (less than 2 weight percent), O (less than 1 weight percent), N (less than 1 weight percent), S (less than 1 weight percent), and Cl (less than 1 weight percent).

Cu which is highly electromigration-resistant is electroplated from plating solutions that contain additives conventionally used to produce bright, ductile, and low-stress plated deposits.

It is an object of the present invention to electroplate conductors of Cu such as interconnect wiring without leaving a seam or a void in the center of the conductor.

It is a further object of the present invention to electroplate conductors of Cu with substantially uniform filling thickness where the conductors have a difference in widths such as less than 1 micron and greater than 10 microns. The depth to width ratio of a conductor may be equal to or greater than 1. The depth to width ratio of a via may exceed 1.

It is a further object of the present invention to lower the manufacturing cost of integrated circuits by the combined effects of 1) blanket deposition of Cu by electrolytic plating, 2) dual damascene fabrication (an approach in which two levels of metallization are fabricated in a single blanket-deposition step), and 3) the ability to planarize the upper surface by processes such as chemical mechanical polishing.

Brief Description of the Drawings

These and other features, objects, and advantages of the present invention will become apparent upon consideration of the following detailed description of the invention when read in conjunction with the drawing in which:

Figures 1-5 are cross-sectional views of intermediate structures illustrating the formation of interconnection wiring.

Figure 6 shows multi-level wiring patterns formed with one plating step.

Figure 7 illustrates early stages of deposition with the deposition rate deep within the feature being greater than the deposition rate outside of the features.

Figure 8 shows late stages of deposition with the deposition rate inside of the features being greater than the deposition rate outside of the features.

Figure 9 illustrates early stages of deposition with the deposition rate inside of the features being slower than the deposition rate outside of the features.

Figure 10 shows late stages of deposition with the

deposition rate inside of the features being slower than the deposition rate outside of the features.

Figure 11 illustrates early stages of deposition with the deposition rate being the same inside and outside of the features.

Figure 12 shows late stages of deposition with the deposition rate being the same inside and outside of the features.

Figure 13 shows a cross-sectional view of a sequence of plating profiles.

Figure 14 shows a cross-sectional view of a feature plated electrolytically using a plating bath without additives.

Figure 15 shows a cross-sectional view of a feature plated electrolytically using a plating bath with additives.

Figure 16 is a cross-sectional view of a substrate having both submicron and wide cavities to be plated.

Figure 17 is a cross-sectional view of the substrate of Figure 16 which has been subsequently plated in a wafer immersion-type plating cell.

Figure 18 is a cross-sectional view of the substrate of Figure 16 which has been subsequently plated in a meniscus-type plating cell (cup plater) where the wafer surface is brought into contact with the upper surface or meniscus of the electrolyte.

Figures 19 a-d are a grain orientation map, grain contrast map, inverse pole figure and (111) pole figure of the same region for a 1 micron thick plated Cu film. The grain size is approximately 1.4 microns and the crystallographic texture is random.

Figures 20 a-d are a grain orientation map, grain contrast map, inverse pole figure and (111) pole figure of the same region for a 1 micron thick PVD (physical vapor deposition, magnetron sputter deposited) Cu film. The grain size is approximately 0.4 microns and this film has a strong (111)/(100) crystallographic texture.

Figures 21a and 21b show the change in resistance versus time (hours) for plated Cu versus a) CVD Cu and b) PVC Cu films. The change in resistance is related to the amount of electromigration damage in the Cu line. Clearly plated Cu has a much improved electromigration behavior than either CVD or PVD Cu. The activation energy for plated Cu is 1.1-1.3 eV while that for PVD Cu is considerably less (0.7-0.8 eV).

Figures 22-26 are cross-sectional views illustrating through-mask plating on a planar base.

Figures 27-31 are cross-sectional views illustrating through-mask plating on an excavated base.

Figures 32-35 are cross-sectional views illustrating blanket plating followed by pattern etching.

Detailed Description of the Embodiments

A Damascene plating process is one in which plating is done over the entire wafer surface and is followed by a planarization process that isolates and defines the features. Plating is preceded by the deposition of a plating base over the entire wiring pattern that has been defined lithographically. Layers that improve adhesion and prevent conductor/insulator interactions and diffusion are deposited between the plating base and the insulator. A schematic representation of the process is shown in Figs. 1-5. The insulator layer (Si oxide, polymer) 1 cladded by etch/planarization layers (Si nitride) 2 and 7 is first deposited on the wafer 8; a resist pattern 3 is formed on the cladded insulator and transferred to the insulator; a barrier material 4 and a seed layer (Cu) 5 are subsequently deposited, and Cu 6 is electroplated so that all features are filled; the structure is brought to its final shape as shown in Fig. 5 by

planarization. It is possible to define lithographically multiple levels of patterns onto the insulator as shown in Fig. 6; in this cost-saving fabrication method, the same sequence of layer deposition is followed.

In order to avoid the formation of a void or seam in Cu 6, the rate of electroplating should be higher at low or deep points within the feature than elsewhere. This is illustrated in Figs. 7-12 where three possible cases of metal deposition are described. In the first case shown in Figs. 7 and 8, metal deposition within features 11 by using additives to the plating bath is faster than outside feature 11 at point 12 and results in void-free and seamless deposits (superfilling) shown in Fig. 8. The preferential deposition in the interior of features may be due to lower transport rates of additives at those locations which in turn leads to an increase in the local rate of Cu deposition. Specifically at interior corners, the rate of additive transport is lowest thus the rate of Copper deposition is highest. In the second case shown in Figs. 9 and 10, metal deposition within features 14 is slower than outside the feature 14 at point 15 and results in voids and high-resistivity lines or vias because deposition within low points 16 of features 14 is from a bath with higher degree of depletion of the depositing ion. The higher degree of ion depletion gives rise to a locally elevated overpotential in the plating bath for the deposition reaction. In the third case shown in Figs. 11 and 12, deposition rates

everywhere, inside feature 17 and outside feature 17 at point 18, are equal (conformal filling) because there is no local ion depletion in the liquid plating bath and because the additives and their beneficial effects (preferential deposition in interior features) are missing. Although nearly acceptable deposits can be obtained by conformal filling, a seam 19 in Cu metal 6 is inevitable in lines and vias with a high aspect ratio. In a reentrant profile, conformed filling is not forgiving and will result in a void. It is evident that plating with superfilling as shown in Figs. 7 and 8 is the required and preferred method for Damascene processing. Electrolytic plating from appropriately formulated solutions is one of the best ways to accomplish the type of deposition shown in Figs. 7 and 8. Superfilling and its relevance to Cu metallization is totally unknown; for example, in the publication by Li et al. cited above, Li et al. stated that the via filling capability of electrolytic Cu plating is "fair-poor."

Superfilling by the use of additives in the plating bath makes it possible to create void-free and seamless lines and vias even if the lithographic process produces features or cavities 22 in a dielectric layer 1 that are narrower at the top than at the bottom as shown in Fig. 13. Electroplating according to the invention herein is one of the best ways by which void-free and seamless lines and vias can be accomplished. Other methods of deposition such as CVD which

at best generate conformal profiles inevitably lead to gross defects especially when lithographic imperfections of this kind are present i.e., features or cavities 22 in a dielectric 1 that are narrower at the top than at the bottom such that sidewall 23 may form an angle with a vertical reference line 24 with respect to the top surface 26 in the range from 0 to 20° as shown by arrow 27.

Copper plating from solutions incorporating additives conventionally used to produce level deposits on a rough surface can be used to accomplish superfilling required to fill sub-micron cavities. One suitable system of additives is the one marketed by Enthone-OMI, Inc., of New Haven, Connecticut and is known as the SelRex Cubath M system. The above additives are referred to by the manufacturer as MHy. Another suitable system of additives is the one marketed by LeaRonal, Inc., of Freeport, New York, and is known as the Copper Gleam 2001 system. The additives are referred to by the manufacturer as Copper Gleam 2001 Carrier, Copper Gleam 2001-HTL, and Copper Gleam 2001 Leveller. And another suitable system of additives is the one marketed by Atotech USA, Inc., of State Park, Pennsylvania, and is known as the Cupracid HS system. The additives in this system are referred to by the manufacturer as Cupracid Brightener and Cupracid HS Basic Leveller.

Examples of specific additives which may be added to a

bath in the instant invention are described in several patents. U.S. patent 4,110,176, which issued on August 29, 1978, to H-G Creutz deceased et al., entitled "Electrodeposition of Copper" described the use of additives to a plating bath such as poly alkanol quaternary-ammonium salt which formed as a reaction product to give bright, highly ductile, low stress and good leveling copper deposits from an aqueous acidic copper plating bath which patent is incorporated herein by reference.

U.S. patent 4,376,685, which issued on March 15, 1983, to A. Watson, entitled "Acid Copper Electroplating Baths Containing Brightening and Leveling Additives," described additives to a plating bath such as alkylated polyalkyleneimine which formed as a reaction product to provide bright and leveled copper electrodeposits from an aqueous acidic bath which patent is incorporated herein by reference.

U.S. patent 4,975,159, which issued on December 4, 1990, to W. Dahms, entitled "Aqueous Acidic Bath for Electrochemical Deposition of a Shiny and Tear-free Copper Coating and Method of Using Same," described adding to an aqueous acidic bath combinations of organic additives including at least one substituted alkoxylated lactam as an amide-group-containing compound in an amount to optimize the brightness and ductility of the deposited copper, which patent is incorporated herein

by reference. In U.S. patent 4,975,159, Table I lists a number of alkoxylated lactams which may be added to a bath in the instant invention. Table II lists a number of sulfur-containing compounds with water-solubilizing groups such as 3-mercaptopropane-1-sulfonic acid which may be added to a bath in the instant invention. Table III lists organic compounds such as polyethylene glycol which may be added to a bath as surfactants in the instant invention.

U.S. patent 3,770,598, which issued on November 6, 1973, to H-G Creutz, entitled "Electrodeposition of Copper from Acid Baths," describes baths for obtaining ductile, lustrous copper containing therein dissolved a brightening amount of the reaction product of polyethylene imine and an alkylating agent to produce a quaternary nitrogen, organic sulfides carrying at least one sulfonic group, and a polyether compound such as polypropylene glycol, which patent is incorporated herein by reference.

U.S. patent 3,328,273, which issued on June 27, 1967, to H-G Creutz et al., entitled "Electrodeposition of Copper from Acidic Baths," describes copper sulfate and fluoborate baths for obtaining bright, low-stress deposits with good leveling properties that contain organic sulfide compounds of the formula $XR_1-(S_n)-R_2-SO_3H$, where R_1 and R_2 are the same or different and are polymethylene groups or alkyne groups containing 1-6 carbon atoms, X is hydrogen or a sulfonic

group, and n is an integer of 2-5 inclusive, which patent is incorporated herein by reference. Additionally these baths may contain polyether compounds, organic sulfides with vicinal sulphur atoms, and phenazine dyes. In U.S. patent 3,328,273, Table I lists a number of polysulfide compounds which may be added to a bath in the instant invention. Table II lists a number of polyethers which may be added to a bath in the instant invention.

Additives may be added to the bath for accomplishing various objectives. The bath may include a copper salt and a mineral acid. Additives may be included for inducing in the conductor specific film microstructures including large grain size relative to film thickness or randomly oriented grains. Also, additives may be added to the bath for incorporating in the conductor material molecular fragments containing atoms selected from the group consisting of C, O, N, S and Cl whereby the electromigration resistance is enhanced over pure Cu. Furthermore, additives may be added to the bath for inducing in the conductor specific film microstructures including large grain size relative to film thickness or randomly oriented grains, whereby the electromigration behavior is enhanced over non-electroplated Cu.

Figure 14 shows a cross-sectional view of the cavity-filling behavior of a plating solution containing 0.3 M cupric sulfate and 10% by volume sulfuric acid of the prior

art. Plating has been interrupted before complete cavity filling to measure deposit thickness at various locations of the feature thus determining the type of filling. It is seen that conformal deposits of Cu 30 are obtained. However, a deposit obtained by the same solution to which chloride ion and MHy additive have been added, exhibits superfilling as shown in Figure 15. The deposition rate deep within the feature is higher than elsewhere, and finally the deposit of Cu 36 shown in Fig. 15 will be void-free and seamless due to higher plating rates inside the feature than outside the feature. MHy concentrations that produce superfilling are in the range from about 0.1 to about 2.5 percent by volume. Chloride ion concentrations are in the range from 10 to 300 ppm.

Similar superfilling results are obtained from a solution containing cupric sulfate in the rate from 0.1 to 0.4M, sulfuric acid in the range from 10 to 20% by volume, chloride in the range from 10 to 300 ppm, and LeaRonal additives Copper Gleam 2001 Carrier in the range from 0.1 to 1% by volume, Copper Gleam 2001-HTL in the range from 0.1 to 1% by volume, and Copper Gleam 2001 Leveller in the range 0 to 1% by volume. Finally, similar superfilling results are obtained from a solution containing cupric sulfate, sulfuric acid, and chloride in the ranges mentioned above and Atotech additives Cupracid Brightener in the range from 0.5 to 3% by volume and Cupracid HS Basic Leveller in the range from 0.01 to 0.5% by

volume.

The plating processes described thus far with additives produce superfilling of submicron, high-aspect-ratio features or cavities when performed in conventional plating cells, such as paddle plating cells described in U.S. patents 5,516,412, 5,312,532, which issued on May 17, 1994 to P. Andricacos et al., and U.S. patent 3,652,442. However, a further benefit described below is realized when the process is performed in a plating cell in which the substrate surface is held in contact only with the free surface of the electrolyte, for example a cup plating cell described in U.S. patent 4,339,319, which issued July 13, 1982, to S. Aigo, which is incorporated herein by reference. The benefit here is the superfilling of wide cavities in the range from 1 to 100 microns, which may be present among the narrow (submicron) features or cavities.

In a plating cell in which the substrate is submerged in the electrolyte, wide features in the range from 1 to 100 microns will fill more slowly than do narrow features having a width less than 1 micron, such as about 0.1 and above; hence wide features necessitate both a longer plating time and a longer polishing time to produce a planarized structure with no dimples or depressions on the top plated surface.

In contrast in a cup plating cell, when the substrate surface to be plated is held in contact with the meniscus of

the electrolyte during plating, cavities of greatly different widths such as less than 1 micron and greater than 10 microns are filled rapidly and evenly at the same rate.

The meniscus of the electrolyte is the curved upper surface of a column of liquid. The curved upper surface may be convex such as from capillarity or due to liquid flow such as from an upwelling liquid.

Figure 16 is a cross-sectional view of a substrate 60 which may have an upper layer of dielectric 61 such as silicon dioxide having surface features or cavities 62 and 63 formed therein for damascene wiring. Cavities 62 may have a width less than one micron and cavity 63 may have a width in the range from 1 to 100 microns. A liner 64 may provide adhesion to dielectric 61 and provide a diffusion barrier to metals subsequently plated. Liner 64 may be conductive to act as a plating base for electroplating or an additional plating base layer may be added.

Figure 17 is a cross-sectional view of substrate 60 having an electrodeposit of metal 66 sufficient to fill cavities 62 and to fill the wide cavity 63 which was plated in an immersion-type cell. In Figure 17, wide feature 63 fills slower than narrow or submicron features 62. The upper surface 67 has a dip 68 over feature 63 with respect to the average height of metal 66.

In Figures 17 and 18, like references are used for functions corresponding to the apparatus of Figs. 16 and 17.

Figure 18 is a cross-sectional view of substrate 60 having an electrodeposit of metal 66 which may be Cu sufficient to fill cavities 62 and to fill wide cavity 63 which was plated in a meniscus-type cup plating cell. As shown in Figure 18, the substrate may be placed in contact with the surface of the bath. The bath may be flowed at the surface of the bath.

In Figure 18, wide feature 63 fills as fast as narrow features 62. The upper surface 69 has a very little dip over feature 63 with respect to the average height of metal 66. Accordingly, we describe a mode of the invention in which the plating is done in a cup plater to achieve even superfilling of narrow and wide features. It is believed that the superior performance of meniscus plating is due to the higher concentration and perhaps different orientation of the surface-active additive molecules at the air-liquid surface. Though these molecules may begin to redistribute when the substrate is introduced, residual effects probably persist throughout the plating period, several minutes in duration.

The electroplated Cu metal 66 shown in Figs. 16 and 17 consists substantially of Cu and may also contain small amounts of atoms and/or molecular fragments of C (less than 2

weight percent), with O (less than 1 weight percent), N (less than 1 weight percent), S (less than 1 weight percent), or Cl (less than 1 weight percent). These additional components apparently originate from the decomposition of additives and are subsequently incorporated in the deposit 66 in the probable form of molecular fragments rather than atoms. Chlorine is co-absorbed due to its synergistic role in activating additive action. As a result, it is believed that these inclusions reside in the grain boundaries and in so doing, they do not affect the resistivity of the plated metal. Indeed, measurements of the resistivity of the plated Cu yield values lower than 2 $\mu\Omega$cm. It is also believed that the same molecules by virtue of the fact that they reside at grain boundaries of Cu render the electromigration resistance of electroplated Cu much better than that of pure Cu that has been deposited by other processes.

The grain size of electroplated Cu is generally larger than that produced by other Cu deposition techniques (see Figures 19 a-d and 20 a-d). Figures 19 a-d are, respectively, a grain orientation map, grain contrast map, inverse pole figure and (111) pole figure of the same region for a 1 micron thick plated Cu film. The grain size is approximately 1.4 microns and the crystallographic texture is random. Figures 20 a-d are, respectively, a grain orientation map, grain contrast map, inverse pole figure and (111) pole figure of the same region for a 1 micron thick PVD Cu film. The grain size

is approximately 0.4 microns and this film has a strong (111)/(100) crystallographic texture.

The crystallographic orientation (also known as texture) of plated Cu is substantially more random than that of non-plated Cu films (see Figures 19 a-d and 20 a-d). This random orientation is indicated by the uniform distribution of grains in the inverse pole figure or the (111) pole figure (see Figures 19 a-d). This is substantially different from that seen for non-plated Cu films. For example, see Figures 20 a-d, where there is substantial (100) and (111) texture in this PVD Cu film.

The electromigration resistance of electroplated Cu and pure Cu is a function of the activation energy as measured by the methods referred to in MRS Bulletin, Volume XVIII, No. 6 (June 1993), and Volume XIX, No. 8 (August 1994), which are incorporated herein by reference. The activation energy of electroplated Cu is equal to or greater than 1.0 eV. In addition, Figures 21a and 21b show a comparison of the drift velocity of plated versus a PVD film. Clearly, the plated Cu shows little change in resistance over time whereas the PVD Cu film resistance increases dramatically. The change in resistance is related to the amount of electromigration damage in the Cu line. Clearly plated Cu has a much improved electromigration behavior than does PVC Cu. The activation energy for plated Cu is 1.1-1.3 eV while that for PVD Cu is

considerably less (0.7-0.8 eV).

The value of the present invention extends beyond implementation in damascene structures. The increased resistance to electromigration, associated with the presence of atoms and/or molecular fragments containing C, O, N, S, and Cl, is similarly beneficial in conductor elements that are fabricated by through-mask plating on a planar base as shown in Figs. 22-26, by through-mask plating on an excavated base as shown in Figs. 22 and 27-31, or by blanket plating followed by patterned etching as shown in Figs. 22, 23 and 32-35.

The process for through-mask plating on a planar base is shown in Figs. 22-26. Fig. 22 shows an insulating layer 1. Fig. 23 shows a seed layer (Cu) 5 formed over insulating layer 1. A barrier material 4 (not shown) may be placed as a layer between insulating layer 1 and seed layer 5. Fig. 24 shows resist 71 which has been patterned over seed layer 5. Fig. 25 shows Cu 6 after electroplating through resist 71. Fig. 26 shows the structure of Fig. 25 with resist 71 removed and with seed layer 5 removed where not protected by Cu 6. Fig. 26 shows a patterned layer of Cu 6 over the patterned seed layer 5.

The process for through-mask plating on an excavated base is shown in Figs. 22 and 27-31. Fig. 22 shows an insulating layer 1. Fig. 27 shows a channel 72 formed in insulating

layer 1. Fig. 28 shows a seed layer (Cu) 5 formed over insulating layer 1. A barrier material 4 (not shown) may be formed underneath seed layer (Cu) 5. Fig. 29 shows resist 71 which has been patterned over seed layer 5. Fig. 30 shows Cu 6 in channel 72 and over seed layer 5 which was deposited by plating through mask or resist 71. Fig. 31 shows Cu 6 with resist 71 removed and with seed layer 5 removed where not protected by Cu 6. It is noted that the superfilling attribute of the plating process of this invention makes it possible to fill cavities or features in the excavated base without remnant voids or seams.

The process for blanket plating followed by pattern etching is shown in Figs. 22, 23 and 32-35 for forming patterned lines on an insulating layer. Fig. 22 shows an insulating layer 1. Fig. 23 shows a barrier layer 4 formed over insulating layer 1. A seed layer (Cu) 5 is formed on the upper surface of barrier layer 4. A blanket layer 76 of Cu is formed as shown in Fig. 32 by electroplating over seed layer 5. A layer of resist 71 is formed over blanket layer 76 and lithographically patterned as shown in Fig. 33. Fig. 34 shows blanket layer 76 patterned by etching or removing by other processes where not protected by resist 71. Fig. 35 shows the patterned blanket layer 76 with resist 71 removed.

In Figures 2-15 and 22-35, like references are used for functions corresponding to the apparatus of an earlier Fig. or

of Fig. 1.

While there has been described and illustrated a process for fabricating an interconnect structure on an electronic device and a Cu conductor having electromigration resistance due to atoms and/or molecular fragments of C, O, N, S, and Cl, and specific microstructural features such as large grains size relative to film thickness and a random crystallographic orientation, it will be apparent to those skilled in the art that modifications and variations are possible without deviating from the broad scope of the invention which shall be limited solely by the scope of the claims appended hereto.

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Claims:

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

1. A process for fabricating an interconnect structure on an electronic device with void-free seamless conductors comprising the steps of:

forming an insulating material on a substrate,

lithographically defining and forming recesses for lines and/or via in said insulating material in which interconnection conductor material will be deposited,

forming a conductive layer on said insulating material serving as a plating base,

depositing said conductor material by electroplating from a bath containing additives, and

planarizing the resulting structure to accomplish electrical isolation of individual lines and/or vias.

2. The process of claim 1 wherein said step of depositing includes depositing Cu as said conductor material.

3. The process of claim 2 further including the step of adding additives to said bath for incorporating in said conductor material positive but small amounts of atoms and/or molecular fragments containing atoms selected from the group consisting of C (less than 2 weight percent), O (less than 1

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weight percent), N (less than 1 weight percent), S (less than 1 weight percent), and Cl (less than 1 weight percent).

4. The process of claim 2 further including the step of adding additives to said bath for inducing in said conductor specific film microstructures including large grain size relative to film thickness and/or randomly oriented grains.

5. The process of claim 2 further including the step of adding additives to said bath for incorporating in said conductor material molecular fragments containing atoms selected from the group consisting of C, O, N, S and Cl whereby the electromigration resistance is enhanced over pure Cu.

6. The process of claim 2 further including the step of adding additives to said bath for inducing in said conductor specific film microstructures including large grain size relative to film thickness and/or randomly oriented grains whereby the electromigration behavior is enhanced over non-electroplated Cu.

7. The process of claim 2 further including the step of electroplating from a bath containing agents conventionally used for producing bright, level deposits on rough surfaces.

8. The process of claim 7 wherein the depth to width

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ratio of a conductor is equal to or greater than 1.

9. The process of claim 7 wherein the depth to width ratio of a via exceeds 1.

10. The process of claim 2 further including the step of electroplating from a solution containing additives conventionally used to deposit bright, level, ductile, and low-stress deposits.

11. The process of claim 10 wherein the depth to width ratio of a conductor is equal to or greater than 1.

12. The process of claim 1 wherein said step of depositing further includes the step of placing the upper surface of said substrate in contact with the surface of said bath.

13. The process of claim 12 wherein said step of depositing further includes flowing said bath at said surface of said bath.

14. The process of claim 1 wherein said step of depositing further includes the step of electroplating using a cup plater.

15. The process of claim 1 further including the step of

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electroplating from a plating solution comprising of a copper salt, a mineral acid, and one or more additives selected from the group consisting of an organic sulfur compound with water solubilizing groups, a bath-soluble high-molecular-weight oxygen-containing compound, a bath-soluble polyether compound, or a bath-soluble organic nitrogen compound that may also contain at least one sulfur atom.

16. The process of claim 15 wherein said plating solution contains small amounts of a chloride ion in the range from 10 to 300 parts per million.

17. The process of claim 15 wherein said Cu salt is cupric sulfate.

18. The process of claim 15 wherein said mineral acid is sulfuric acid.

19. The process of claim 15 wherein said organic sulfur compound carries at least one sulfonic group.

20. The process of claim 15 wherein said organic sulfur compound has at least two sulfur atoms that are vicinal.

21. The process of claim 20 wherein said organic sulfur compound has at least two sulfur atoms that are vicinal and carries at least one terminal sulfonic group.

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22. The process of claim 15 wherein said organic sulfur compound is selected from the group consisting of mercaptopropane sulfonic acid, thioglycolic acid, mercaptobenzthiozol-S-propansulfonic acid and ethylenedithiodipropyl sulfonic acid, dithiocarbamic acid, alkali metal salts of said compounds, and amine salts of said compounds.

23. The process of claim 15 wherein said organic sulfur compound has the formula $X-R_1-(S_n)-R_2-SO_3H$ where the R groups are the same or different and contain at least one carbon atom, X is selected from the group consisting of a hydrogen and a sulfonic group, and n is 2-5 inclusive.

24. The process of claim 15 wherein said oxygen-containing compound is selected from the group consisting of polyethylene glycol, polyvinyl glycol, polypropylene glycol, and carboxymethylcellulose.

25. The process of claim 15 wherein said organic nitrogen compound is selected from the group containing pyridines and substituted pyridines, amides, quaternary ammonium salts, imines, phthalocyanines and substituted phthalocyanines, phenazines, and lactams.

26. A process for fabricating an interconnect structure on an electronic device comprising the steps of:

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depositing a seed layer on a substrate having insulating regions and conductive regions,

forming a patterned resist layer on said seed layer,

electroplating conductor material on said seed layer not covered by said patterned resist from a bath containing additives, and

removing said patterned resist.

27. The process of claim 26 wherein said step of depositing includes depositing Cu as said conductor material.

28. The process of claim 27 further including the step of adding additives to said bath for incorporating in said conductor material small amounts of atoms and/or molecular fragments containing atoms selected from the group consisting of C (less than 2 weight percent), O (less than 1 weight percent), N (less than 1 weight percent), S (less than 1 weight percent), and Cl (less than 1 weight percent).

29. The process of claim 27 further including the step of adding additives to said bath for inducing in said conductor specific film microstructures including large grain size relative to film thickness and/or randomly oriented grains.

30. The process of claim 27 further including the step of adding additives to said bath for incorporating in said

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conductor material molecular fragments containing atoms selected from the group consisting of C, O, N, S and Cl whereby the electromigration resistance is enhanced over pure Cu.

31. The process of claim 27 further including the step of adding additives to said bath for inducing in said conductor specific film microstructures including large grain size relative to film thickness and/or randomly oriented grains whereby the electromigration behavior is enhanced over non-electroplated Cu.

32. The process of claim 27 further including the step of electroplating from a bath containing agents conventionally used for producing smooth, level deposits on rough surfaces.

33. The process of claim 32 wherein the depth to width ratio of a conductor exceeds 1.

34. The process of claim 32 wherein the depth to width ratio of a via exceeds 1.

35. The process of claim 27 further including the step of electroplating from a solution containing additives conventionally used to deposit bright, level, ductile, or low-stress deposits.

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36. The process of claim 35 wherein the depth to width ratio of a conductor exceeds 1.

37. The process of claim 26 wherein said step of depositing further includes the step of placing the upper surface of said substrate in contact with the surface of said bath.

38. The process of claim 37 wherein said step of depositing further includes flowing said bath at said surface of said bath.

39. The process of claim 26 wherein said step of depositing further includes the step of electroplating using a cup plater.

40. The process of claim 16 further including the step of electroplating from a plating solution comprising of a copper salt, a mineral acid, and one or more additives selected from the group consisting of an organic sulfur compound with water solubilizing groups, a bath-soluble high-molecular-weight oxygen-containing compound, a bath-soluble polyether compound, or a bath-soluble organic nitrogen compound that may also contain at least one sulfur atom.

41. The process of claim 40 wherein said plating

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solution contains small amounts of a chloride ion in the range from 10 to 300 parts per million.

42. The process of claim 40 wherein said Cu salt is cupric sulfate.

43. The process of claim 41 wherein said mineral acid is sulfuric acid.

44. The process of claim 40 wherein said organic sulfur compound carries at least one sulfonic group.

45. The process of claim 40 wherein said organic sulfur compound has at least two divalent sulfur atoms that are vicinal.

46. The process of claim 45 wherein said organic sulfur compound has at least two sulfur atoms that are vicinal and carries at least one terminal sulfonic group.

47. The process of claim 40 wherein said organic sulfur compound is selected from the group consisting of mercaptopropane sulfonic acid, thioglycolic acid, mercaptobenzthiozol-S-propansulfonic acid and ethylenedithiodipropyl sulfonic acid, dithiocarbamic acid, alkali metal salts of said compounds, and amine salts of said compounds.

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48. The process of claim 45 wherein said organic sulfur compound has the formula $X-R_1-(S_n)-R_2-SO_3H$ where the R groups are the same or different and contain at least one carbon atom, X is selected from the group consisting of a hydrogen and a sulfonic group, and n is 2-5 inclusive.

49. The process of claim 40 wherein said oxygen-containing compound is selected from the group consisting of polyethylene glycol, polyvinyl glycol, polypropylene glycol, and carboxymethylcellulose.

50. The process of claim 40 wherein said organic nitrogen compound is selected from the group containing pyridines and substituted pyridines, amides, quaternary ammonium salts, imines, phthalocyanines and substituted phthalocyanines, phenazines, and lactams.

51. A process for fabricating an interconnect structure on an electronic device with void-free seamless conductors comprising the steps of:

depositing an insulating material on a substrate,

lithographically defining and forming lines and/or vias in which interconnection conductor material will be deposited,

forming a conductive layer serving as a plating base,

forming a patterned resist layer on said plating base,

depositing said conductor material by electroplating from a bath containing additives, and

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removing said patterned resist.

52. The process of claim 51 wherein said step of depositing includes depositing Cu as said conductor material.

53. The process of claim 52 further including the step of adding additives to said bath for incorporating in said conductor material small amounts of atoms and/or molecular fragments containing atoms selected from the group consisting of C (less than 2 weight percent), O (less than 1 weight percent), N (less than 1 weight percent), S (less than 1 weight percent), and Cl (less than 1 weight percent).

54. The process of claim 52 further including the step of adding additives to said bath for inducing in said conductor specific film microstructures including large grain size relative to film thickness and/or randomly oriented grains.

55. The process of claim 52 further including the step of adding additives to said bath for incorporating in said conductor material molecular fragments containing atoms selected from the group consisting of C, O, N, S and Cl whereby the electromigration resistance is enhanced over pure Cu.

56. The process of claim 52 further including the step

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of adding additives to said bath for inducing in said conductor specific film microstructures including large grain size relative to film thickness and/or randomly oriented grains whereby the electromigration behavior is enhanced over non-electroplated Cu.

57. The process of claim 52 further including the step of electroplating from a bath containing agents conventionally used for producing smooth, level deposits on rough surfaces.

58. The process of claim 57 wherein the depth to width ratio of a conductor exceeds 1.

59. The process of claim 57 wherein the depth to width ratio of a via exceeds 1.

60. The process of claim 52 further including the step of electroplating from a solution containing additives conventionally used to deposit bright, level, ductile, or low-stress deposits.

61. The process of claim 60 wherein the depth to width ratio of a conductor exceeds 1.

62. The process of claim 51 wherein said step of depositing further includes the step of placing the upper surface of said substrate in contact with the surface of said

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bath.

63. The process of claim 62 wherein said step of depositing further includes flowing said bath at said surface of said bath.

64. The process of claim 51 wherein said step of depositing further includes the step of electroplating using a cup plater.

65. The process of claim 51 further including the step of electroplating from a plating solution comprising of a copper salt, a mineral acid, and one or more additives selected from the group consisting of an organic sulfur compound with water solubilizing groups, a bath-soluble high-molecular-weight oxygen-containing compound, a bath-soluble polyether compound, or a bath-soluble organic nitrogen compound that may also contain at least one sulfur atom.

66. The process of claim 65 wherein said plating solution contains small amounts of a chloride ion in the range from 10 to 300 parts per million.

67. The process of claim 65 wherein said Cu salt is cupric sulfate.

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68. The process of claim 65 wherein said mineral acid is sulfuric acid.

69. The process of claim 65 wherein said organic sulfur compound carries at least one sulfonic group.

70. The process of claim 65 wherein said organic sulfur compound has at least two divalent sulfur atoms that are vicinal.

71. The process of claim 70 wherein said organic sulfur compound has at least two sulfur atoms that are vicinal and carries at least one terminal sulfonic group.

72. The process of claim 65 wherein said organic sulfur compound is selected from the group consisting of mercaptopropane sulfonic acid, thioglycolic acid, mercaptobenzthiozol-S-propansulfonic acid and ethylenedithiodipropyl sulfonic acid, dithiocarbamic acid, alkali metal salts of said compounds, and amine salts of said compounds.

73. The process of claim 65 wherein said organic sulfur compound has the formula $X-R_1-(S_n)-R^2-SO_3H$ where the R groups are the same or different and contain at least one carbon atom, X is selected from the group consisting of a hydrogen and a sulfonic group, and n is 2-5 inclusive.

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74. The process of claim 65 wherein said oxygen-containing compound is selected from the group consisting of polyethylene glycol, polyvinyl glycol, polypropylene glycol, and carboxymethylcellulose.

75. The process of claim 65 wherein said organic nitrogen compound is selected from the group containing pyridines and substituted pyridines, amides, quaternary ammonium salts, imines, phthalocyanines and substituted phthalocyanines, phenazines, and lactams.

76. A process of fabricating an interconnect structure on an electronic device comprising the steps of:

depositing a seed layer on a substrate having insulating regions and conductive regions,

forming a blanket layer of conductor material on said seed layer from a bath containing additives,

forming a patterned resist layer on said blanket layer,

removing said conductor material where not covered by said patterned resist, and

removing said patterned resist.

77. The process of claim 76 wherein said step of depositing includes depositing Cu as said conductor material.

78. The process of claim 77 further including the step of adding additives to said bath for incorporating in said

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conductor material small amounts of atoms and/or molecular fragments containing atoms selected from the group consisting of C (less than 2 weight percent), O (less than 1 weight percent), N (less than 1 weight percent), S (less than 1 weight percent), and Cl (less than 1 weight percent).

79. The process of claim 77 further including the step of adding additives to said bath for inducing in said conductor specific film microstructures including large grain size relative to film thickness and/or randomly oriented grains.

80. The process of claim 77 further including the step of adding additives to said bath for incorporating in said conductor material molecular fragments containing atoms selected from the group consisting of C, O, N, S, and Cl whereby the electromigration resistance is enhanced over pure Cu.

81. The process of claim 77 further including the step of adding additives to said bath for inducing in said conductor specific film microstructures including large grain size relative to film thickness and/or randomly oriented grains whereby the electromigration behavior is enhanced over non-electroplated Cu.

82. The process of claim 77 further including the step

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of electroplating from a bath containing agents conventionally used for producing smooth, level deposits on rough surfaces.

83. The process of claim 82 wherein the depth to width ratio of a conductor exceeds 1.

84. The process of claim 82 wherein the depth to width ratio of a via exceeds 1.

85. The process of claim 77 further including the step of electroplating from a solution containing additives conventionally used to deposit bright, level, ductile, or low-stress deposits.

86. The process of claim 85 wherein the depth to width ratio of a conductor exceeds 1.

87. The process of claim 76 wherein said step of depositing further includes the step of placing the upper surface of said substrate in contact with the surface of said bath.

88. The process of claim 87 wherein said step of depositing further includes flowing said bath at said surface of said bath.

89. The process of claim 76 wherein said step of

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depositing further includes the step of electroplating using a cup plater.

90. The process of claim 76 further including the step of electroplating from a plating solution comprising of a copper salt, a mineral acid, and one or more additives selected from the group consisting of an organic sulfur compound with water solubilizing groups, a bath-soluble high-molecular-weight oxygen-containing compound, a bath-soluble polyether compound, or a bath-soluble organic nitrogen compound that may also contain at least one sulfur atom.

91. The process of claim 90 wherein said plating solution contains small amounts of a chloride ion in the range from 10 to 300 parts per million.

92. The process of claim 90 wherein said Cu salt is cupric sulfate.

93. The process of claim 90 wherein said mineral acid is sulfuric acid.

94. The process of claim 90 wherein said organic sulfur compound carries at least one sulfonic group.

95. The process of claim 90 wherein said organic sulfur

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compound has at least two divalent sulfur atoms that are vicinal.

96. The process of claim 95 wherein said organic sulfur compound has at least two sulfur atoms that are vicinal and carries at least one terminal sulfonic group.

97. The process of claim 90 wherein said organic sulfur compound is selected from the group consisting of mercaptopropane sulfonic acid, thioglycolic acid, mercaptobenzthiozol-S-propansulfonic acid and ethylenedithiodipropyl sulfonic acid, dithiocarbamic acid, alkali metal salts of said compounds, and amine salts of said compounds.

98. The process of claim 90 wherein said organic sulfur compound has the formula $X-R_1-(S_n)-R_2-SO_3H$ where the R groups are the same or different and contain at least one carbon atom, X is selected from the group consisting of a hydrogen and a sulfonic group, and n is 2-5 inclusive.

99. The process of claim 90 wherein said oxygen-containing compound is selected from the group consisting of polyethylene glycol, polyvinyl glycol, polypropylene glycol, and carboxymethylcellulose.

100. The process of claim 90 wherein said organic

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nitrogen compound is selected from the group containing pyridines and substituted pyridines, amides, quaternary ammonium salts, imines, phthalocyanines and substituted phthalocyanines, phenazines, and lactams.

101. A conductor for use in interconnections on an electronic device comprising:

Cu including small amounts of a material in said Cu selected from the group consisting of C (less than 2 weight percent), O (less than 1 weight percent), N (less than 1 weight percent), S (less than 1 weight percent), and Cl (less than 1 weight percent) formed by electroplating from a bath containing additives.

102. The conductor of claim 101 further including specific film microstructures including large grain size relative to film thickness and/or randomly oriented grains.

103. The conductor of claim 101 wherein said small amounts of material include atoms and/or molecular fragments.

104. The conductor of claim 101 wherein said conductor has an activation energy for electromigration equal to or grater than 1.0 eV and further includes specific film microstructures including large grain size relative to film thickness and/or randomly oriented grains whereby the electromigration behavior is enhanced over non-electroplated

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Cu.

105. A conductor for use in interconnections on an electronic device comprising:

a dielectric layer having a substantially planar upper surface and having a pattern of recesses therein,

said recesses having a width at said upper surface less than one micrometer,

said recesses filled with continuous metal from a bath containing additives by electroplating, said metal comprising copper.

106. The conductor of claim 105 wherein said recesses have a depth to width ratio equal to or greater than 1.

107. The conductor of claim 105 wherein said recesses have a conductive layer on said recesses on said dielectric layer to serve as a plating base.

108. The conductor of claim 105 further including a metal liner between said conductive layer and said dielectric layer in said recesses.

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