



(51) International Patent Classification:
G11C 17/18 (2006.01) *G11C 17/16* (2006.01)

(21) International Application Number:
PCT/US2011/042092

(22) International Filing Date:
28 June 2011 (28.06.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/359,155 28 June 2010 (28.06.2010) US
12/849,862 4 August 2010 (04.08.2010) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

[Continued on next page]

(54) Title: NON-VOLATILE MEMORY WITH SPLIT WRITE AND READ BITLINES

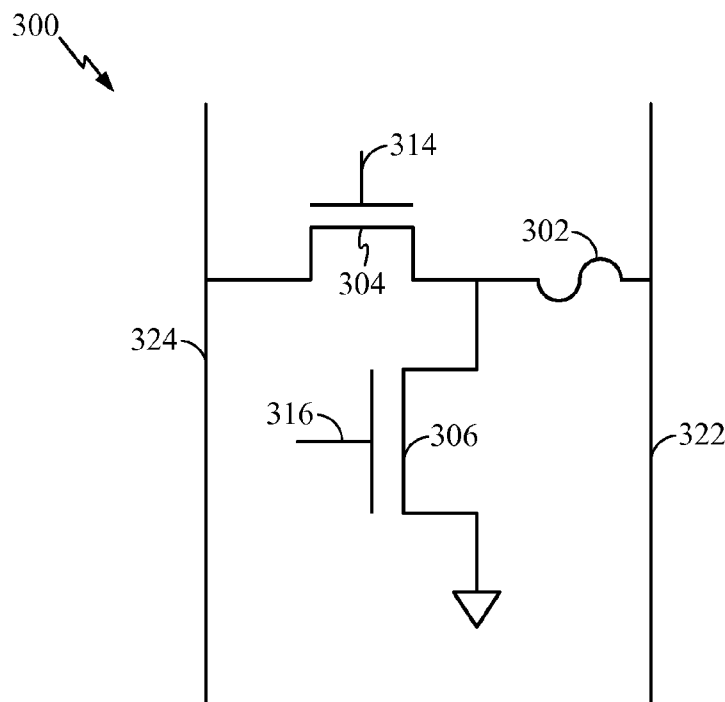


FIG. 3

(57) Abstract: Read and write operations of a non-volatile memory (NVM) bitcell have different optimum parameters resulting in a conflict during design of the NVM bitcell. A single bitline in the NVM bitcell prevents optimum read performance. Read performance may be improved by splitting the read path and the write path in a NVM bitcell between two bitlines. A read bitline of the NVM bitcell has a low capacitance for improved read operation speed and decreased power consumption. A write bitline of the NVM bitcell has a low resistance to handle large currents present during write operations. A memory element of the NVM bitcell may be a fuse, anti-fuse, eFUSE, or magnetic tunnel junction. Read performance may be further enhanced with differential sensing read operations.



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- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*
- Published:**
- *with international search report (Art. 21(3))*