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A SELF ALIGNED CHANNEL DOPING METHOD FOR HIGH SPEED MOS TRANSISTORS

BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

This invention relates to the formation of relatively heavy doping concentrations only in the lightly doped drain regions for metal oxide semiconductor, MOS, field effect transistors having sub micron channel lengths. More particularly the invention relates to a method of forming lightly doped drain and halo regions for a device formed in a heavily doped semiconductor well.

(2) DESCRIPTION OF THE RELATED ART

U.S. Pat. No. 5,270,234 to Huang et al. describes a method of channel doping for sub micron MOS devices using channel doping before the formation of the gate electrode. Planarization is accomplished using chemical mechanical

polishing.

Non uniformly doped channel regions is discussed in the paper "Source-to-Drain Nonuniformly Doped Channel (NUDC) MOSFET Structures for High Current Drivability and Threshold Voltage Controllability" by Y. Okumara et al., IEEE Transactions on Electron Devices, Vol. 39, No. 11, November 1992, pages 2541-2552.

This invention uses ion implantation to form lightly doped drain and halo regions after the gate electrode has been formed to produce relatively high doping concentrations only in the lightly doped drain regions.

SUMMARY OF THE INVENTION

When MOS, metal oxide semiconductor, field effect transistors are scaled to dimensions producing sub micron channel lengths short channel effects become apparent and must be dealt with. Increased doping levels are required to suppress leakage current but higher doping concentrations lead to larger junction capacitance with adverse affects on circuit performance.

It is a principle objective of this invention to provide a self-aligned lightly doped drain, LDD, doping method which provides high doping concentrations only in the lightly doped drain region thereby avoiding an increase in junction capacitance.

This objective is achieved by forming a window in a dielectric layer wherein the window is formed over a lightly doped drain, LDD, region of a semiconductor substrate where the LDD will be formed. Spacers are formed on the sidewalls of the window. The gate electrode is then formed and the spacers are removed leaving openings between the dielectric layer and the gate electrode. Ion implantation through these openings changes the doping level of the region of the semiconductor directly below the openings thereby forming a lightly doped drain region. The

substrate is then annealed and a halo region of semiconductor type having an opposite polarity to the lightly doped drain region is formed using ion implantation and again annealed.

The dielectric layer is then removed and spacers are formed on the sidewalls of the gate electrode. Source and drain regions are then formed using conventional methods. This leaves LDD regions of semiconductor material having relatively high doping concentrations without having high doping concentrations at the junctions of the device. Increased junction capacitance is avoided and improved device performance can be realized.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a cross section of a semiconductor substrate showing a window in a first and second dielectric layers covered by a third dielectric layer.

Fig. 2 shows a cross section of the semiconductor substrate of Fig. 1 showing spacers of third dielectric material formed on the sidewalls of the window.

Fig. 3 shows a cross section of the semiconductor substrate of Fig. 1 with a gate oxide layer formed in the window and a blanket polysilicon gate electrode layer formed on the substrate.

Fig. 4 shows a cross section of the semiconductor substrate of Fig. 1 after etchback of the polysilicon gate electrode layer has formed the polysilicon gate electrode.

Fig. 5 shows a cross section of the semiconductor substrate of Fig. 1 after the gate electrode has been formed, the spacers have been etched away, and the lightly doped drain and halo regions have been formed.

Fig. 6 shows a cross section of the semiconductor substrate after spacers have been formed on the gate electrode and source and drain regions have been formed.

Fig. 7 shows a cross section of a semiconductor substrate showing a window in a first, second, and third dielectric layers covered by a fourth dielectric layer.

Fig. 8 shows a cross section of the semiconductor substrate of Fig. 7 showing spacers of fourth dielectric material formed on the sidewalls of the window.

Fig. 9 shows a cross section of the semiconductor substrate of Fig. 7 with a gate oxide layer formed in the window and a blanket polysilicon gate electrode layer formed on the substrate.

Fig. 10 shows a cross section of the semiconductor substrate of Fig. 7 after the gate electrode has been formed, the spacers have been etched away, and the lightly doped drain and halo regions have been formed.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Refer now to Figs. 1-6, there is shown an embodiment of the method of self aligned LDD/halo doping of this invention. Fig. 1 shows a cross section of a semiconductor substrate 10. This embodiment describes an N channel metal oxide semiconductor device formed in a P type semiconductor substrate. Those skilled in the art will recognize that the method will work equally well for a device formed in a P type device well, or for a P channel metal oxide semiconductor device formed in an N type substrate or an N type device well.

In this embodiment the semiconductor substrate 10 is silicon having a P type impurity concentration of between about 1 X 10^{15} and 1 X 10^{18} $/cm^3$. The impurity concentration of the silicon substrate is chosen to be large enough so that leakage current will be suppressed in MOS devices having channel lengths less than 1 micron. Next, as shown in Fig. 1, a first dielectric layer 12, such as silicon dioxide having a thickness of between about 100 and 500 Angstroms, is formed on the silicon substrate 10. A second dielectric layer 14, such as Si_3N_4 having a thickness of between about 1000 and 3000 Angstroms, is then formed on the layer of silicon dioxide 12. A first opening 15, having sidewalls, is formed in the first dielectric layer 12 and

second dielectric layer 14 using conventional lithographic and etching techniques thereby exposing a first region 17 of the semiconductor substrate 10. A third dielectric layer 16 is then formed conformally over the second dielectric layer 14 covering the sidewalls of the first opening 15 and the first region 17 of the semiconductor substrate 10. In this embodiment the third dielectric layer 16 is silicon dioxide formed using chemical vapor deposition of tetra-ethyl-ortho-silicate, TEOS, having a thickness of between about 500 and 2000 Angstroms.

As shown in Fig. 2, the TEOS silicon dioxide layer is then etched back leaving first oxide spacers 19 on the sidewalls of the first opening 15 and a gate region 21 of the semiconductor substrate 10 between the first oxide spacers 19. As shown in Fig. 3, a gate oxide layer 18, such as thermally grown silicon dioxide having a thickness of between about 40 and 100 Angstroms, is formed on the gate region 21. A blanket layer of gate electrode material 20, such as polysilicon, is then formed on the semiconductor substrate. The gate electrode material 20 is then etched back leaving a gate electrode 23 formed on the gate oxide layer 18, see Fig. 4. The gate electrode 23 is formed of a material such as polysilicon having a doping level of between about 1×10^{19} and 5×10^{20} /cm^3.

As shown in Fig. 5, the first oxide spacers are then etched away forming second openings 25 between the first 12 and second 14 dielectric layers and the gate electrode 23 and exposing regions of the semiconductor substrate 10 adjacent to the gate oxide layer 18. Lightly doped drain regions 22 are then formed in the semiconductor substrate using a ion implantation beam through the second openings 25 between the first 12 and second 14 dielectric layers and the gate electrode 23. The semiconductor substrate is then annealed at a temperature of between about 850° C and 950° C for between about 10 and 60 minutes. The halo regions 24 are then formed directly below the lightly doped drain regions 22 using an ion implantation beam through the second openings 25 between the first 12 and second 14 dielectric layers and the gate electrode 23. The semiconductor substrate is again annealed. In this embodiment the lightly doped drain regions 22 are formed using an ion implantation beam of Phosphorus ions and are silicon having an N^- type concentration of between about 1×10^{17} and 5×10^{18} /cm^3. The halo regions are formed using an ion implantation beam of Boron ions and have a P^- type concentration of between about 5×10^{17} and 5×10^{18} /cm^3. The halo will have a deeper junction depth than the lightly doped drain regions.

As shown in Fig. 6 the first dielectric layer and second dielectric layer are then removed and second oxide spacers 26 are then formed on the sidewalls of the gate electrode 23. The second oxide spacers 26 are formed over the lightly doped drain regions 22 and mask the lightly doped drain regions 22 when the source and drain regions 28 are formed. The source and drain regions 28 are then formed using conventional ion implantation methods.

This embodiment provides relatively heavily doped halo regions to suppress leakage current for MOS devices with channel lengths less than one micron. The halo regions are located only under the second oxide spacers 26 and increase in junction capacitance is avoided.

Refer now to Figs. 7-10 and 6, there is shown another embodiment of the method of self aligned channel doping of this invention. In this embodiment the semiconductor substrate 10 is silicon having a P type impurity concentration of between about 1×10^{15} and 1×10^{18} /cm^3. The impurity concentration of the silicon substrate is chosen to be large enough so that leakage current will be suppressed in MOS devices having channel lengths less than 1 micron. Next, as shown in Fig. 7, a first dielectric layer 12, such as silicon dioxide having a thickness of between about 100 and 500 Angstroms, is formed

on the silicon substrate 10. A second dielectric layer 14, such as Si_3N_4 having a thickness of between about 1000 and 3000 Angstroms or either doped or undoped polysilicon having a thickness of between about 1000 and 3000 Angstroms, is then formed on the layer of silicon dioxide 12. A third dielectric layer 30, such as silicon dioxide having a thickness of between about 500 and 2000 Angstroms, is then formed on the second dielectric layer 14. A first opening 15, having sidewalls, is formed in the first dielectric layer 12, second dielectric layer 14, and third dielectric layer 30 using conventional lithographic and etching techniques thereby exposing a first region 17 of the semiconductor substrate 10. A fourth dielectric layer 16 is then formed conformally over the third dielectric layer 30 covering the sidewalls of the first opening 15 and the first region 17 of the semiconductor substrate 10. In this embodiment the fourth dielectric layer 16 is silicon dioxide formed using chemical vapor deposition of tetra-ethyl-ortho-silicate, TEOS, having a thickness of between about 500 and 2000 Angstroms.

As shown in Fig. 8, the TEOS silicon dioxide layer is then etched back leaving first oxide spacers 19 on the sidewalls of the first opening 15 leaving a gate region 21 of the semiconductor substrate 10 between the first oxide spacers 19. As shown in Fig. 9, a gate oxide layer 18, such

as thermally grown silicon dioxide having a thickness of between about 40 and 100 Angstroms, is formed on the gate region 21. A blanket layer of gate electrode material 20, such as polysilicon, is then formed on the semiconductor substrate. The gate electrode material 20 is then etched back leaving a gate electrode 23 formed on the gate oxide layer 18, see Fig. 10. The gate electrode 23 is formed of a material such as polysilicon having a doping concentration of between about 1 X 10^{19} and 5 X 10^{20} /cm^3.

As shown in Fig. 10, the first oxide spacers are then etched away forming second openings 25 between the first 12 and second 14 dielectric layers and the gate electrode 23 and exposing regions of the semiconductor substrate 10 adjacent to the gate oxide layer 18. Lightly doped drain regions 22 are then formed in the semiconductor substrate using a ion implantation beam through the through the second openings 25 between the first 12 and second 14 dielectric layers and the gate electrode 23. The semiconductor substrate is then annealed at a temperature of between about 850° C and 950° C for between about 10 and 60 minutes. The halo regions 24 are then formed directly below the lightly doped drain regions 22 using an ion implantation beam through the second openings 25 between the first 12 and second 14 dielectric layers and the gate electrode 23. The semiconductor substrate is again annealed. In this

embodiment the lightly doped drain regions 22 are formed using an ion implantation beam of Phosphorus ions and are silicon having an N^- type concentration of between about 1 X 10^{17} and 5 X 10^{18} /cm^3. The halo regions are formed using an ion implantation beam of Boron ions and have a P^- type concentration of between about 5 X 10^{17} and 5 X 10^{18} /cm^3. The halo will have a deeper junction depth than the lightly doped drain regions.

As shown in Fig. 6 the first dielectric layer and second dielectric layer are then removed and second oxide spacers 26 are then formed on the sidewalls of the gate electrode 23. The source and drain regions 28 are then formed as described in the preceding embodiment.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of self aligned lightly doped drain doping, comprising the steps of:

providing a semiconductor substrate having a first surface;

forming a first dielectric layer on said first surface of said semiconductor substrate;

forming a second dielectric layer on said first dielectric layer;

forming a first opening having sidewalls in said first dielectric layer and said second dielectric layer thereby exposing a first region of said first surface of said semiconductor substrate, wherein said first region of said first surface of said semiconductor substrate consists of a gate region of said first surface of said semiconductor substrate and a second region of said first surface of said semiconductor substrate;

forming a third dielectric layer on said second dielectric layer, said sidewalls of said first opening, said gate region of said first surface of said semiconductor, and said second region of said first surface of said semiconductor substrate;

etching back said third dielectric layer thereby forming first spacers on said sidewalls of said first opening and exposing said gate region of said first surface of said semiconductor substrate;

forming a gate oxide layer on said gate region of said first surface of said semiconductor substrate;

forming a layer of polysilicon on said gate oxide layer, said second dielectric layer, and said first spacers;

etching back said layer of polysilicon thereby forming a polysilicon gate electrode having sidewalls on said gate oxide layer;

etching away said first spacers thereby forming second openings and exposing said second region of said first surface of said semiconductor substrate;

forming lightly doped drain regions in said semiconductor substrate under said second region of said first surface of said semiconductor substrate using ion implantation through said second openings;

forming halo regions under said lightly doped drain regions using ion implantation through said second openings;

removing said first dielectric layer and said second dielectric layer after forming said lightly doped drain regions and said halo regions;

forming second spacers on said sidewalls of said polysilicon gate electrode after removing said first dielectric layer and said second dielectric layer; and

forming source and drain regions in said semiconductor substrate, after forming said second spacers, using ion implantation.

2. The method of claim 1 wherein said semiconductor substrate is P type silicon having an impurity concentration of between about 1 X 10^{15} and 1 X 10^{18} /cm^3.

3. The method of claim 2 wherein said lightly doped drain regions are N^- type silicon having an impurity concentration of between about 1 X 10^{17} and 5 X 10^{18} /cm^3, said halo regions are P^- type silicon having an impurity concentration of between about 5 X 10^{17} and 5 X 10^{18} /cm^3, and said source and drain regions are N^+ type silicon having an impurity concentration of between about 1 X 10^{19} and 5 X 10^{20} /cm^3.

4. The method of claim 1 wherein said semiconductor substrate is N type silicon having an impurity concentration of between about 1 X 10^{17} and 5 X 10^{18} /cm^3.

5. The method of claim 4 wherein said lightly doped drain regions are P^- type silicon having an impurity concentration of between about 1 X 10^{17} and 5 X 10^{18} /cm^3, said halo regions are N^- type silicon having an impurity concentration of between about 5 X 10^{17} and 5 X 10^{18} /cm^3, and said source and drain regions are P^+ type silicon having an impurity concentration of between about 1 X 10^{19} and 5 X 10^{20} /cm^3.

6. The method of claim 1 wherein said first dielectric layer is silicon dioxide having a thickness of between about 100 and 500 Angstroms.

7. The method of claim 1 wherein said second dielectric layer is silicon nitride having a thickness of between about 1000 and 3000 Angstroms.

8. The method of claim 1 wherein said third dielectric layer is silicon dioxide formed using chemical vapor deposition of tetra-ethyl-ortho-silicate and has a thickness of between about 500 and 2000 Angstroms.

9. The method of claim 1 wherein said second spacers are silicon dioxide.

10. A method of self aligned lightly doped drain doping, comprising the steps of:

providing a semiconductor substrate having a first surface;

forming a first dielectric layer on said first surface of said semiconductor substrate;

forming a second dielectric layer on said first dielectric layer;

forming a third dielectric layer on said second dielectric layer;

forming a first opening having sidewalls in said first dielectric layer, said second dielectric layer, and said third dielectric layer thereby exposing a first region of said first surface of said semiconductor substrate, wherein said first region of said first surface of said semiconductor substrate consists of a gate region of said first surface of said semiconductor substrate and a second region of said first surface of said semiconductor substrate;

forming a fourth dielectric layer on said second dielectric layer, said sidewalls of said first opening, said gate region of said first surface of said semiconductor, and said second region of said first surface of said semiconductor substrate;

etching back said fourth dielectric layer thereby forming first spacers on said sidewalls of said first opening and exposing said gate region of said first surface of said semiconductor substrate;

forming a gate oxide layer on said gate region of said first surface of said semiconductor substrate;

forming a layer of polysilicon on said gate oxide layer, said third dielectric layer, and said first spacers;

etching back said layer of polysilicon thereby forming a polysilicon gate electrode having sidewalls on said gate oxide layer;

etching away said first spacers thereby forming second openings and exposing said second region of said first surface of said semiconductor substrate;

forming lightly doped drain regions in said semiconductor substrate under said second region of said first surface of said semiconductor substrate using ion implantation through said second openings;

forming halo regions under said lightly doped drain regions using ion implantation through said second openings;

removing said first dielectric layer, said second dielectric layer, and said third dielectric layer after forming said lightly doped drain regions and said halo regions;

forming second spacers on said sidewalls of said polysilicon gate electrode after removing said first dielectric layer, said second dielectric layer, and said third dielectric layer; and

forming source and drain regions in said semiconductor substrate, after forming said second spacers, using ion implantation.

11. The method of claim 10 wherein said semiconductor substrate is P type silicon having an impurity concentration of between about 1×10^{15} and 1×10^{18} /cm^3.

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12. The method of claim 11 wherein said lightly doped drain regions are N^- type silicon having an impurity concentration of between about 1 X 10^{17} and 5 X 10^{18} /cm^3, said halo regions are P^- type silicon having an impurity concentration of between about 5 X 10^{17} and 5 X 10^{18} /cm^3, and said source and drain regions are N^+ type silicon having an impurity concentration of between about 1 X 10^{19} and 5 X 10^{20} /cm^3.

13. The method of claim 10 wherein said semiconductor substrate is N type silicon having an impurity concentration of between about 1 X 10^{15} and 1 X 10^{18} /cm^3.

14. The method of claim 13 wherein said lightly doped drain regions are P^- type silicon having an impurity concentration of between about 1 X 10^{17} and 5 X 10^{18} /cm^3, said halo regions are N^- type silicon having an impurity concentration of between about 5 X 10^{17} and 5 X 10^{18} /cm^3, and said source and drain regions are P^+ type silicon having an impurity concentration of between about 1 X 10^{19} and 5 X 10^{20} /cm^3.

15. The method of claim 10 wherein said first dielectric layer is silicon dioxide having a thickness of between about 100 and 500 Angstroms.

16. The method of claim 10 wherein said second dielectric layer is silicon nitride having a thickness of between about 1000 and 3000 Angstroms.

17. The method of claim 10 wherein said second dielectric layer is polysilicon having a thickness of between about 1000 and 3000 Angstroms.

18. The method of claim 10 wherein said third dielectric layer is silicon dioxide having a thickness of between about 100 and 500 Angstroms.

19. The method of claim 10 wherein said fourth dielectric layer is silicon dioxide formed using chemical vapor deposition of tetra-ethyl-ortho-silicate and has a thickness of between about 500 and 2000 Angstroms.

20. The method of claim 10 wherein said second spacers are silicon dioxide.

ABSTRACT OF THE DISCLOSURE

A SELF ALIGNED CHANNEL DOPING METHOD FOR HIGH SPEED MOS TRANSISTORS

A method of self aligned lightly doped drain/halo doping for suppressing leakage current while avoiding increased junction capacitance in metal oxide semiconductor field effect transistors having sub micron channel lengths. A gate window is formed in a dielectric layer and spacers are formed on the sidewalls of the gate window. After formation of the gate electrode the spacers are etched away and lightly doped drain regions are formed using ion implantation through the openings formed by etching away the spacers. This provides relatively heavy doping concentrations only in the lightly doped drain regions and avoids the increase of junction capacitance.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)

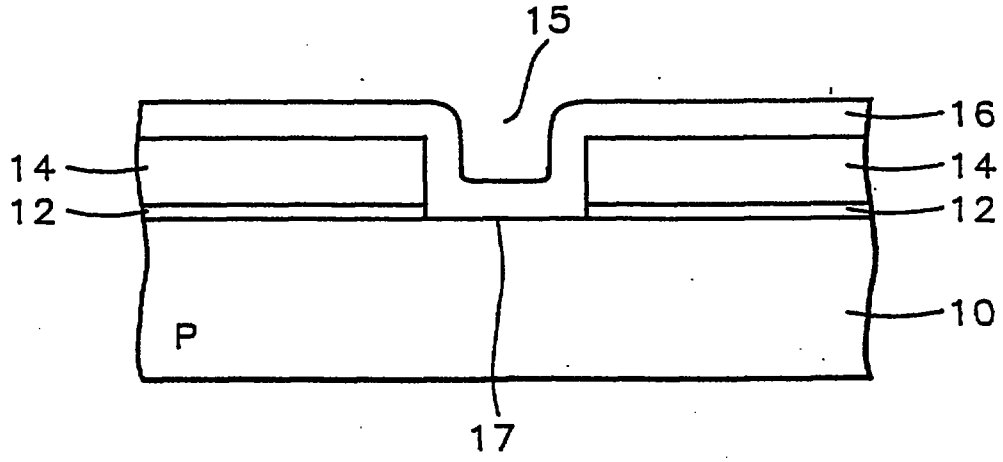


FIG. 1

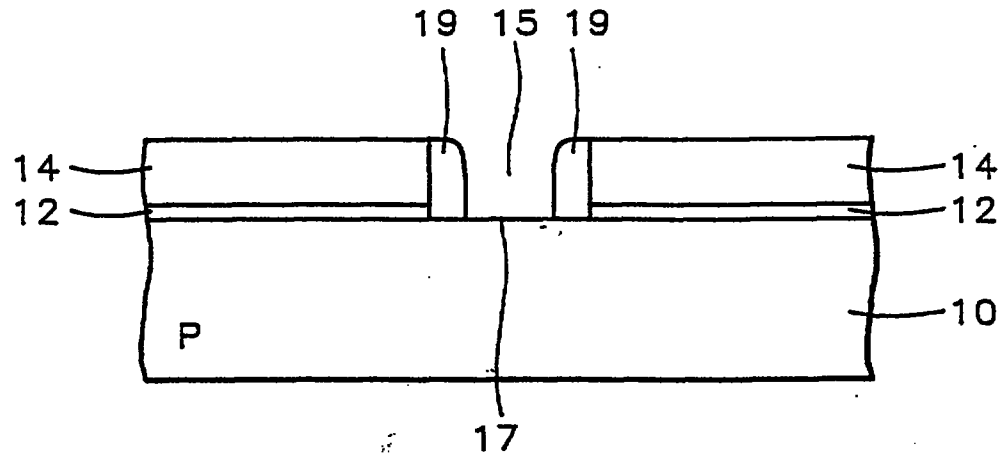


FIG. 2

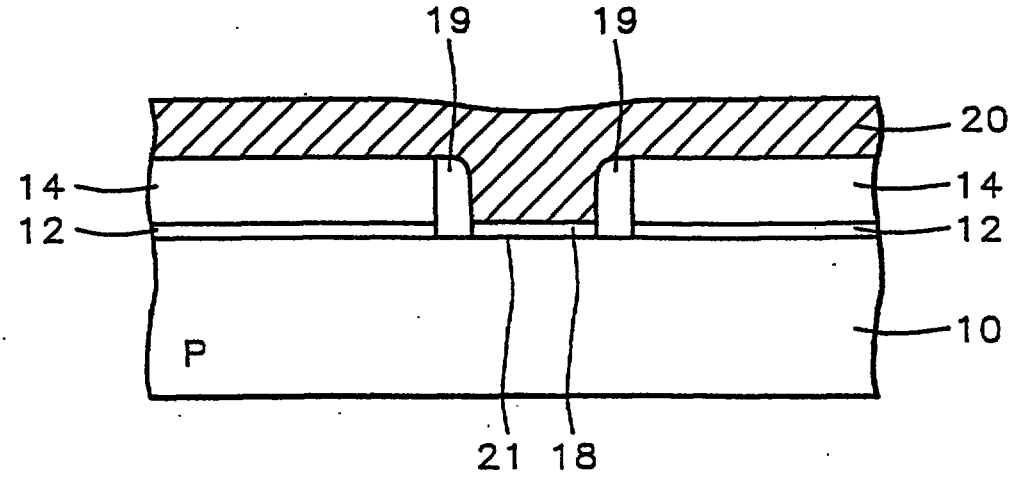


FIG. 3

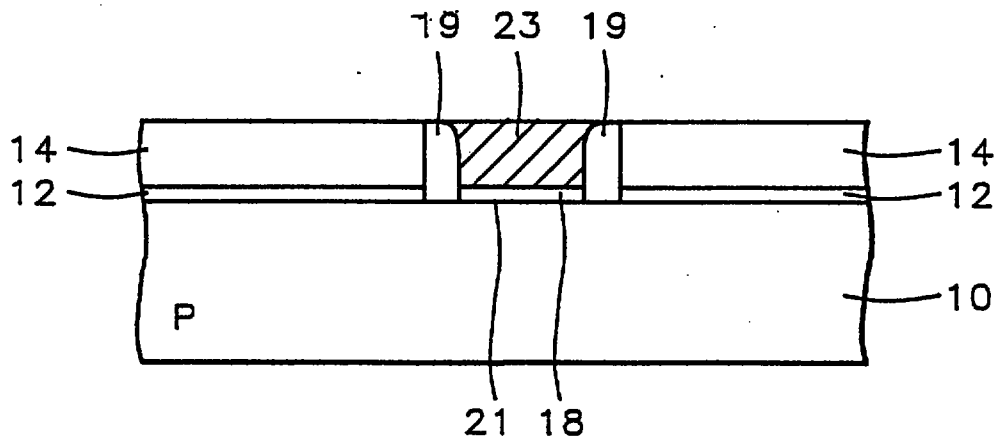


FIG. 4

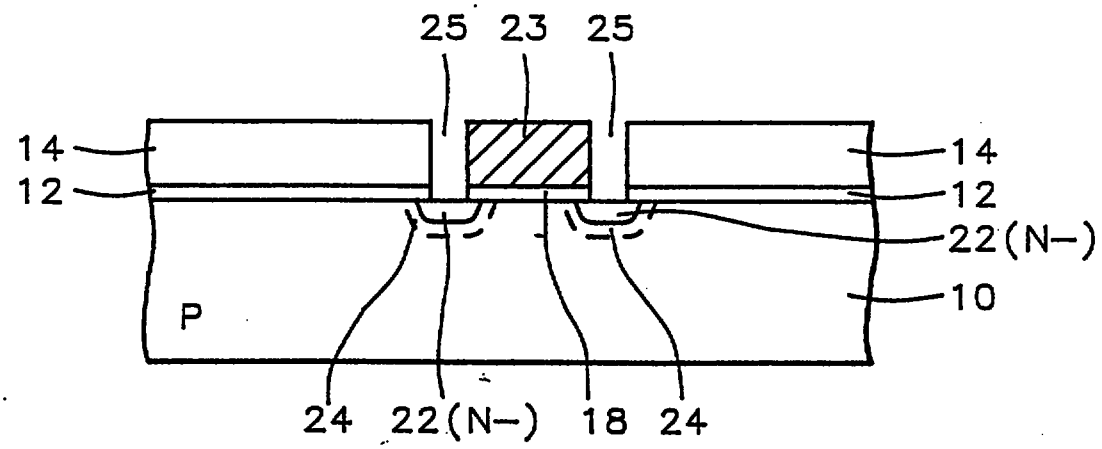


FIG. 5

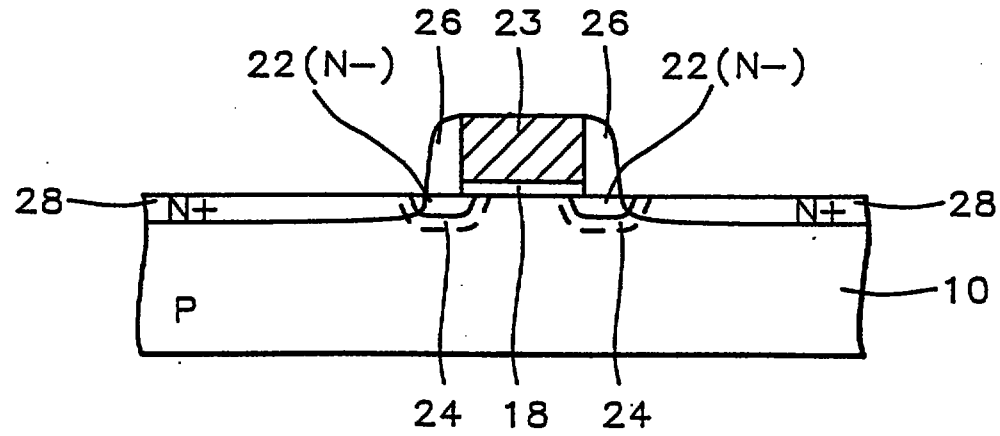


FIG. 6

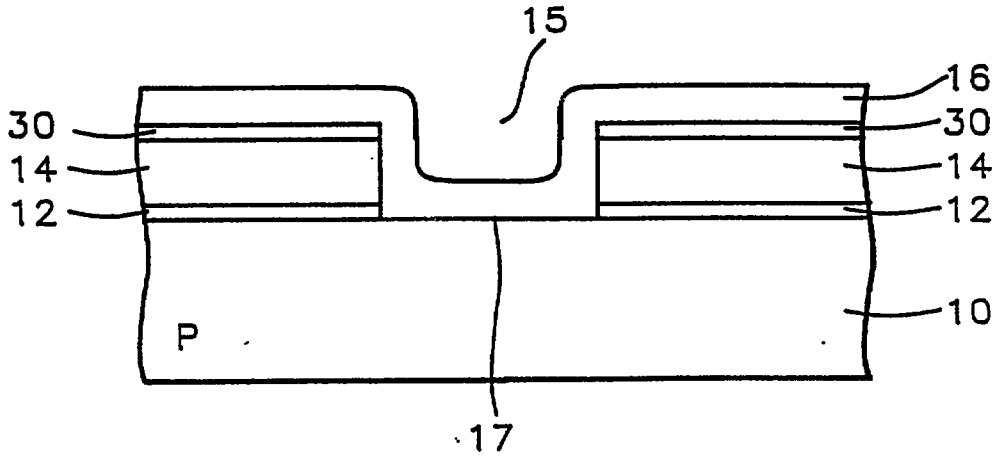


FIG. 7

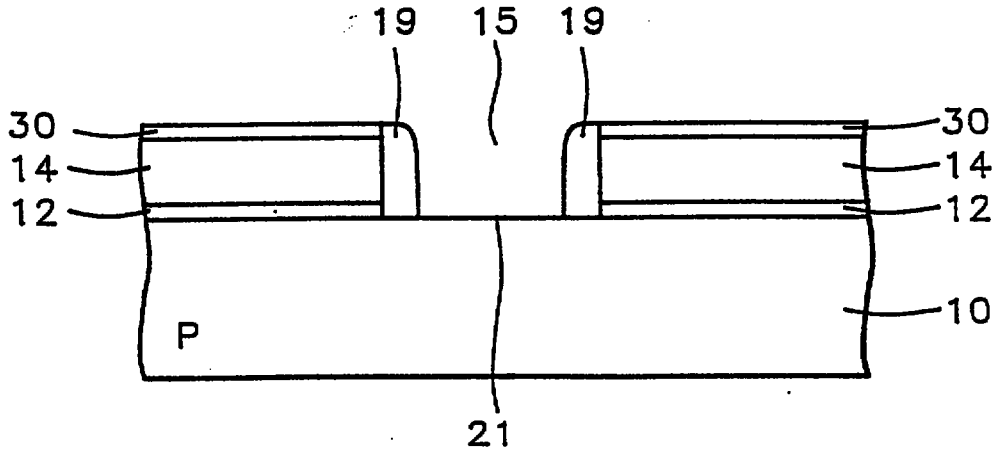


FIG. 8

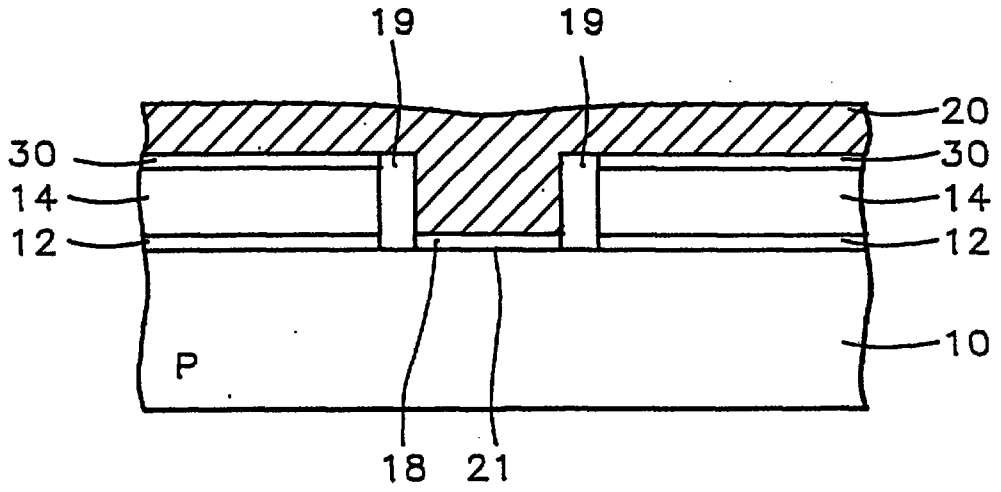

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FIG. 9

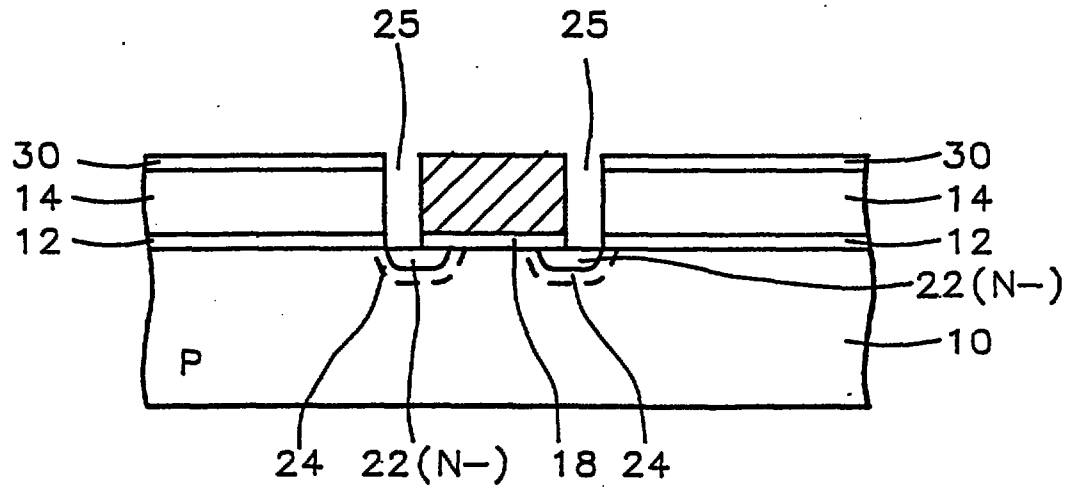

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22(N-)
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P
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22(N-)
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FIG. 10