Claims:

1. A memory management method, comprising:

   identifying, by a Memory Management Unit (MMU), a type of a memory controller externally connected based on configuration information of a Central Processing Unit (CPU);

   based on an address management sub-module and an address area corresponding to the type of the memory controller, determining, by the MMU, an offset address in a manner of table look-up;

   calculating, by the MMU, a logical address of the type of the memory controller based on the offset address; wherein the numbers of external connection channels gated by different types of memory controllers are different;

   wherein the method further comprises:

   receiving, by the MMU, off-chip data sent by a packet memory unit (PMU), wherein the off-chip data comprises a packet descriptor (PD) and a packet (PK);

   extracting data information of the PD;

   co-packing the data information to obtain co-packed data, and deleting a first data in the PK;

   performing shift and concatenations on the co-packed data according to effective data bits, and extracting second data;

   co-packing the data information of the PD in the co-packed data and the extracted second data to obtain target co-packed data; and

   sending the target co-packed data to an off-chip memory for storage.

2. The method according to claim 1, wherein the method further comprises:

   reading, by an address mapping submodule of the MMU, a preset address mapping relationship, and the address mapping relationship is for converting an on-chip logical address into a physical address that can be accepted by a memory chip.

3. The method according to claim 2, wherein the method further comprises:

   performing, according to different application scenarios, a reconfiguration on the preset address mapping relationship by means of the CPU, so as to acquire a reconfigured address mapping relationship corresponding to the application scenario.

4. The method according to claim 1, wherein the method further comprises:

according to an off-chip memory requirement and a structural attribute of the memory controller, a data packet sent by the CPU to the MMU is segmented according to a block unit, wherein the segmented data packets corresponds to block addresses, one data packet corresponds to a plurality of block addresses, and managed address ranges are different when the types of the memory controller are different.

5. The method according to claim 1, wherein the method further comprises:

outputting the PD and the second data at a same time when a data bit length of the PD plus a data bit length of the extracted second data is less than or equal to a bus bit width;

splitting the PD and the second data into first split data and second split data when the data bit length of the PD plus the extracted data bit length of the second data is greater than the bus bit width;

outputting the PD and the first split data;

performing a zero-padding operation on the second split data to obtain zero-padding processed data with a data bit length equal to the bus bit width, and outputting the zero-padding processed data.

6. The method according to any one of claims 1 to 5, wherein the method further comprises:

issuing, by a packet memory unit (PMU), a writing packet;

storing, by the PMU, the writing packet, and sending a write release command to a Traffic Memory management unit (TMMU), and sending, by the TMMU, a Packet Descriptor to a queue management unit (QMU);

issuing, by the QMU, a write command via the TMMU, and transparently transmits the write command to the MMU, and after storing the write command, sending, by the QMU, a write release signal to the TMMU;

issuing, by a command queue, a reading packet command, reading the data corresponding to the reading packet command and returning the data corresponding to the reading packet command to the PMU;

sending, by the TMMU, a read command, and reading the data of the packet descriptor.

7. A memory management apparatus, comprising:

an identification unit, configured to identify, based on configuration information of a central processing unit (CPU), a type of a memory controller externally connected;

a determination unit, configured to determine an offset address in a manner of table look-up based on an address management sub-module and an address area corresponding to the type of the memory controller;

a calculation unit, configured to calculate a logic address of the type of the memory controller based on the offset address, wherein the numbers of external connection channels gated by different types of memory controllers are different;

the memory management apparatus is further configured to:

receive off-chip data sent by a packet memory unit (PMU), wherein the off-chip data comprises a packet descriptor (PD) and a packet (PK);

extract data information of the PD;

co-pack the data information to obtain co-packed data, and delete a first data in the PK;

perform shift and concatenations on the co-packed data according to effective data bits, and extract second data;

co-pack the data information of the PD in the co-packed data and the extracted second data to obtain target co-packed data; and

send the target co-packed data to an off-chip memory for storage.

8. A non-transitory computer-readable storage medium, a computer program is stored in the non-transitory computer-readable storage medium, and the computer program is configured to cause, when executed by a processor, the processor to perform the method as claimed in any one of claims 1 to 6.

9. A controller, comprising a memory and a processor, wherein a computer program is stored in the memory, and the processor is configured to execute the computer program to perform the method as claimed in any one of claims 1 to 6.