

ABSTRACT

(Figure 9)

Method and Apparatus for Transmitting Information
on a Wired-OR Bus

A method and apparatus for use in transmitting information on a wired-OR signal line is described which employs a data transfer protocol exploiting the generally shorter signal settling time occurring following high to low signal voltage transitions than occurs following low to high signal voltage transitions. In accordance with the protocol, the transmission of meaningful information on multiple-driver signal lines is restricted to the assertion of high to low signal voltage transitions. By asserting meaningful information only on high to low transitions, the clock period for the bus may be set based on the voltage settling time resulting from only high to low transitions rather than from arbitrary transitions. As a result, the transmission of meaningful signals are all within the limits of incident wave switching and a high overall information transmission rate is achieved. The amount of information transferable per clock cycle depends upon whether the wired-OR signal line is a single driver line, a multiple driver line wherein events are correlated with commonly observable events, or a multiple driver line wherein events are not correlated with commonly observable events. For single driver lines, one unit of information per clock cycle may be transmitted. For multiple driver lines which are correlated with commonly observable events, one unit of information may be transmitted every two clock cycles. For multiple driver lines which are not correlated with commonly observable events, one unit of information per three clock cycles may be transmitted. Method and apparatus embodiments of the invention are described in particular with reference to a multiprocessor computer system having a latched wired-OR bus.