

Description

This invention relates to circuitry for processing digital signals occurring as serial multi-bit words or samples.

Recent advances in integrated circuit technology have fostered a trend toward converting many analog signal processing systems to digital signal processing systems. The impetus for this trend is greater system reliability, fewer system parts and the potential for simplified automated assembly and parametric adjustments. Specific examples are digital television receivers and audio compact disc players.

There are in general two types of digital processing systems, serial-bit and parallel-bit. The parallel-bit systems are capable of processing signals of greater bandwidth but require more hardware while serial-bit systems are generally simpler but are signal bandwidth limited (at least for economical consumer applications). For the current state of the art of digital signal processing, the bandwidth of video signals require that digital video systems be realized in parallel-bit technology. However, the bandwidth of audio signals, for example, is sufficiently narrow to permit serial-bit digital processing.

Serial digital signals are multi-bit binary samples with respective bits of a given sample occurring sequentially in time, usually with the least significant bit (LSB) occurring first and the most significant bit (MSB) or sign bit occurring last. A sample is a binary number representing a signal amplitude. In a digital serial-bit processing system, the samples are normally processed arithmetically. Signal amplification or attenuation corresponds to sample multiplication and division respectively. Multiplication by powers of two increases the number of bits in the corresponding sample by one bit for each power of two and division essentially reduce the number of bits in the sample. The product of two N-bit samples is a 2N-bit sample. The sum or difference of two N-bit samples is an (N+1)-bit sample.

Typically in a serial-bit digital processing system, samples are sequentially subjected to different ones of the foregoing mathematical functions. Consequently, the number of bits of the processed samples increase and/or decrease. It will readily be appreciated, that since the sample bits occur sequentially, the change in sample bit width creates significant timing difficulties for the system designer. For example, addition requires a particular number of clock pulses per sample operation and multiplication a different number of clock pulses per sample operation.

In view of the above, the present invention provides apparatus for processing serial-bit two's

complement digital signals whose length may vary occurring in equally spaced intervals with all bits of a sample occurring in less than a sample interval, comprising: a serial arithmetic processing unit having an input and an output terminal; a serial shift register having an input, an output and a clock input terminal; characterized by a sign-extend-register having an input, an output, a clock input and a sign-extend signal input terminal and arranging for replicating the sign bit of a sample for the remainder of the sample interval in response to the sign-extend signal; means for serially coupling said serial shift register, said arithmetic processing unit and said sign extend register wherein said arithmetic processing unit is disposed between said registers; means for generating a first clock signal having a first predetermined number of pulses per sample interval, a second clock signal having a second predetermined number of pulses per sample interval and a sign-extend signal occurring at the occurrence of a predetermined sign-bit of said serial-bit digital samples; and means for coupling said first and second clock signals to the clock input terminals of said serial shift register and sign-extend register respectively, and means for coupling said sign-extend signal to said sign-extend input terminal, whereby in operation as a sample is clocked out of the serial shift register, the sign-extend register is arranged to pass the sample to the serial arithmetic processing unit and to extend the sign-bit of the sample for the remaining pulses of the sample interval.

An aspect of the present invention relates to a frame oriented serial-bit digital signal processing system wherein a frame defines the period between two successive N-bit serial samples. Functional elements within the system include a serial register for receiving and outputting the sequential bits of each sample applied thereto in the order of LSB first and MSB last. A latch is serially coupled to the output of the serial register. The serial bits are sequentially passed through the latch in a manner to appropriately justify each sample. The sign bit, upon entering the latch, is retained in the latch to replicate the sign bit state for the remainder of the respective frame interval. The register and sign bit extension apparatus provide a means to absorb varying sample bit-widths in a processing chain with standardized clocking and control signals.

Embodiment of the present invention, given by way of non-limitative example, will now be described with reference to the accompanying drawings, in which:

FIGURE 1 is a block diagram of a serial-bit digital processing element including sign-extend registers embodying the present invention.

FIGURE 2 is a clock timing-waveform diagram illustrating system timing for a serial processor

embodying the invention.

FIGURES 3-8 are block diagrams of serial arithmetic processing elements embodying the present invention.

FIGURE 9A is a partial schematic, partial block diagram of a serial-bit digital envelope detector utilizing the circuitry illustrated in FIGURES 1 and 3-8; and FIGURE 9B is an analog equivalent of the FIGURE 9A apparatus.

The apparatus of FIGURE 1 illustrates the basic form of an embodiment of the invention which will be described with the aid of the clock waveforms illustrated in FIGURE 2. In FIGURE 1, serial digital samples to be processed are applied at terminal 10. These samples occur at a sample rate defined by the waveform ST in FIGURE 2 with the sample bit rate defined by the waveform CLOCK. The number of bits per sample may be N, but in general the resolution of the sample may be less than N-bits. In other words, although each sample may contain N bits, the maximum possible signal sample value may be represented by (N-V)-bits. N and V are both integers but the value of V may vary throughout a system because the maximum possible values of the processed samples may increase or decrease and therefore the number of bits required to define the sample value will increase or decrease. For example, if the number of bits, N, of a sample is 20, but the maximum possible sample value is 255 which may be represented with 8 bits, then V equals 12. If this sample is doubled, the doubled sample value is 510 which requires 9 bits. In this instance, the value of V can be no greater than 11.

The N-V information bits of each serial sample occur, in a series, from least significant bit (LSB) to most significant bit (MSB). The extra V bits are appended to the MSB end of each sample to absorb changing bit widths of processed samples. The samples are presumed to be in two's complement format with the (N-V)th bit representing the sign bit. In order to efficiently process two's complement samples, the sign bit is traditionally constrained to occupy the MSB portion of each respective sample. This condition is achieved by replicating the (N-V)th sign bit in the V subsequent bit positions. In two's complement format, an N-bit sample having V extra MSB's replicating the (N-V)th sign bit of a sample with (N-V) bit resolution has the same numeric value as an (N-V) bit sample.

Referring again to FIGURE 1 assume that an (N-V) bit two's complement sample is applied to terminal 10. This sample is synchronously clocked into the N-stage serial shift register 14 under the control of the clock signal CLOCK N having N clocking pulses. The first clock pulse is synchronized to occur coincidently with the first or least significant sample bit. The sample bits are clocked

into the N-V least significant bit positions of register 14, that is into the register stages closest to the register output connection. The information loaded into the V more significant positions of the register (the register stages nearest the input connection) may be one or zeroes, their values being immaterial. At the end of the Nth clock pulse of CLOCK N, CLOCK N is halted and the sample is stored in the register until the next sample period. In this example, so far, the sign bit has not been replicated into the V-MSB's of the register (or the sample).

For the present ignore element 16 and assume that during the next sample period CLOCK N is again energized for N clock periods and the sample contained in register 14 is coupled in a bit series to the serial arithmetic processing unit SAPU 18. Assume also that SAPU 18 is designed to add a constant represented by more than N-V bits to the current sample. If the sign bit of the current sample is not replicated, an error may result. For example, assume that a two's complement representation of the value eight (01000) is to be added to the current sample. Assume further that N is equal to five, (N-V) is equal to four and the current sample value is minus one and that the V MSB's of the current sample are zero. As defined, the current sample is represented by (01111). The result of adding (01000) to (01111) produces the erroneous result of (10111) or minus nine in two's complement. Alternatively, if the sign bit of the current sample (second bit from the left of the value 01111) is replicated in the MSB, the current sample becomes (11111). When this value is added to (01000) the correct result of (00111) is produced.

Sign bit replication is accomplished by connecting a sign extension latch, 16, serially to the output terminal of register 14. Latch 16 is conditioned by a control signal XND to pass the first N-V-1 sample bits output by register 14 and to latch and hold the (N-V)th sample bit (the sign bit) for the remainder of the sample period. Latch 16 may be of the type designated SN74LS75 "Bistable Latches" available from Texas Instruments Inc., Dallas, Texas. The timing of the control signal XND applied to latch 16 relative to the clock pulses provided by CLOCK N is illustrated in FIGURE 2.

In this example, since latch 16 holds the (N-V)th sample bit for the remainder of the sample period, it will be readily appreciated that the values stored in the V MSB positions of register 12 are immaterial. Note, however, that if the sign bit of the (N-V) bit sample in register 14 has been replicated in the V MSB positions then the onset of the control signal may be delayed to the (N-1)st clock pulse of CLOCK N. In this instance the number of bits defining the sample resolution may change to greater or lesser numbers but the leading edge of

the control pulse XND can be held constant at clock pulse (N-1).

Nominally, the positive going transition of the signal XND will be generated to occur immediately after the clock pulse corresponding to the most significant value bit position of the sample having the least number of value bits in a given system. To accommodate samples defined with a greater number of bits processed by similar circuits in the system, the positive going transition of signal XND is delayed by the appropriate number of clock periods by, for example, flip-flop stages.

The combination of the register 14 and latch 16 will subsequently be designated a sign-extend-shift-register, SXSRR.

The output of the SAPU 18 is coupled to a further SXSRR 20. The SAPU 18 in general will not contain sample storage so SXSRR 20 is provided to accept the sample bits as they are processed and to store the processed bits until the next sample period. If the SAPU 18 processes samples without delay, that is the processing of a respective bit is completed within its corresponding clock period, SXSRR 20 will be clocked by CLOCK N. Alternatively if the processed bits incur bit-time delays in being processed in SAPU 18, SXSRR 20 must be clocked by more than N pulses to properly right justify the sample bits in the register for the next sample period.

Consider that the sample bits incur a delay of M clock pulse periods in being processed in SAPU 18. In order for the LSB of the processed sample to be registered in the LSB position of the N stage SXSRR 20 upon completion of processing the respective sample, SXSRR 20 must be clocked with N+M clock pulses. In FIGURES 1 and 2 CLOCK P provides the appropriate numbers of pulses.

In general, CLOCK P provides a number of pulses per sample period to accommodate the particular SAPU in the system, which has the greatest processing delay. Additional register stages are coupled between other SAPU's (having lesser processing delays) and their corresponding SXSRR's so that a common clock signal CLOCK P may be utilized for at least a majority of processing circuits having processing delays. The number of additional register stages are selected so that the processing delay (in clock pulse periods) plus the additional stages plus N equals the number P.

The apparatus in FIGURE 1 includes an SXSRR at the input and output of the processing element 18. In general, SXSRR 12 will be associated with a preceding processing stage and it is not intended to be implied that an arithmetic processing element embodying the present invention requires both an input and an output SXSRR. In fact, certain processing functions may be serially chained together without intervening SXSRR's.

The system clocks and/or control signals are generated in the control unit 22. Control unit 22 may include an oscillator from which the master clock, CLOCK, is derived. CLOCK N, CLOCK P, sample signal ST and the sign extend control signal XND may all be derived from the master clock signal by conventional counting and gating circuits. One skilled in the art of digital signal processing will readily be able to generate such signals knowing the relationships illustrated in FIGURE 2.

FIGURE 3 illustrates circuitry to multiply a serial sample by a constant value equal to $2^{-(P-N)}$. Shifting all the bits of a sample to one bit position of lesser significance effects a multiplication of the sample by a factor of $\frac{1}{2}$. Shifting all the bits of a sample to N-bit positions of lesser significance effects a scaling or multiplication by 2^{-N} and shifting the bits to (P-N) bit positions of lesser significance effects a multiplication by $2^{-(P-N)}$. Assume that at the beginning of a sample period register 12 contains an N-bit sample. Assume also that SXSRR registers 12 and 25 have equal numbers of stages. SXSRR 12 is clocked by CLOCK N and SXSRR 25 is clocked by CLOCK P with $P > N$. After N clock pulses the sample in SXSRR 12 has been transferred into SXSRR 25. However, CLOCK P continues to run clocking the sample further through SXSRR 25. P-N sample bits are lost off the right end of SXSRR 25. At the end of the burst of CLOCK P pulses, the 2N-P more significant bits of the original N-bit sample occupy the 2N-P LSB positions of register 25. The P-N MSB positions of register 25 are loaded with the replicated sign-bit of the sample from register 12. The value of the sample in register 25 is $2^{-(P-N)}$ times the value of the original N-bit sample due to the change in bit significance. Note that the sign extend latch of register 25 is energized after N-1 clock pulses to replicate the sign bit of the stored sample. Replicating the sign bit in register 25 occurs during the time that the P-N bits from register 12 are clocked out of register 12 to perform the multiplication. For practical implementations of this circuit the number of clock pulses of clock P minus the number of clock pulses of CLOCK N must be less than the number of bits defining the resolution of the original samples or else the shifted samples will be rendered equal to a value of zero.

FIGURE 4 is one embodiment of a stage for delaying a sample by one sample period. The circuit consists of the cascade connection of an SXSRR 12, a (P-N)-stage shift register 26 and SXSRR 27. The value (P-N) is equal to the difference in the number of pulses between CLOCK P and CLOCK N. The number of stages in each of registers 12 and 27 are assumed to be N. The number of stages in the combined registers 26 and 27 is equal to (P-N)+N or P stages. Consequently, P

clock pulses are required to clock the LSB from SXSr 12 into the LSB position of SXSr 27. This is precisely the number of pulses occurring in a burst of CLOCK P pulses in each sample period. Thus, registers 26 and 27 provide a delay of one sample period if they are clocked by CLOCK P. It will be readily appreciated by one skilled in the art of serial digital processing that register 26 may be clocked continuously by the master clock, CLOCK. It will also be appreciated that an N-stage SXSr substituted for registers 26 and 27 and clocked by CLOCK N will effect a one sample period delay for a serial sample.

Next consider that registers 26 and 27 are clocked by CLOCK N. In this instance, at the end of the CLOCK N pulse train the LSB of the sample from SXSr 12 will be in the (P-N)th LSB position of register 27. Essentially, all of the bits of the sample have been shifted to (P-N) more significant bit positions. This shift in bit position significance is equivalent to a multiplication of the sample by $2^{(P-N)}$. Thus, multiplication by multiples of two may be performed by interposing register stages in the signal processing path and division by multiples of two may be performed by adding clock pulses to, for example, the clock signal of a register.

FIGURE 5 illustrates circuitry for summing two serial samples. The signals to be summed (SA and SB) are shown provided by SXSr's 30 and 32 respectively. The samples SA from SXSr 30 and samples SB from SXSr 32 are coupled to the augend/addend input terminals A and B of a full adder 36. Adder 36 may be of the type designated SN74H183 and sold by Texas Instrument Inc., Dallas, Texas. The sum output bits provided by adder 36 are coupled to the "D" type flip-flop 38. Flip-flop 38 is serially interposed in the sum signal path to afford the adder 36 a full bit time to perform each bit sum while providing stable sum bits to subsequent circuit elements.

The carry-out bit from adder 36 is delayed one clock period in the "D" type flip-flop 34 and coupled to the carry-in input terminal CI of adder 36. Flip-flop 34 provides the carry from the sum of each pair of addend/augend sample bits for addition to the sum of the next more significant pair of addend/augend sample bits. Flip-flop 34 is nominally reset to a zero at the beginning of each sample period by the signal ST.

The sum output available from flip-flop 38 is delayed one clock period relative to the input samples. If the output of flip-flop 38 is coupled to the standard N-stage SXSr register clocked by CLOCK N the samples will be multiplied by the factor 2 because of the extra one-bit delay. In order to store the sample sum for the duration of the sample period and to normalize the sums, the output of flip-flop 38 is coupled to the cascade

connection of a (P-N-1) stage register 40 and an N-stage register 42. Flip-flop 38 and register 40 combine to form a register, which when coupled with SXSr 42, functions similar to registers 26 and 27 in FIGURE 4. Clocking flip-flop 38 and register 40 with the signal CLOCK and clocking SXSr 42 with CLOCK P results in each sample sum being appropriately justified in register 42 at the end of each sample period.

FIGURE 6 illustrates a two's complement circuit. Two's complementing is performed by inverting (complementing) the sample bits and adding one unit, that is incrementing the value of the complemented sample by the least significant bit unit value. In FIGURE 6, the sample bits are inverted in inverter 45 and coupled to a standard half-adder 46, such as is illustrated at page 135 of Design of Digital Computers by Hans W. Gschwind (Springer-Verlag, New York, 1967). The output of half-adder 46 is coupled to "D" type flip-flop 38 and the cascade connection of register 40 and SXSr 42 which function in like fashion to the similar combination in FIGURE 5.

The carry-out, Co, from half-adder 46 is delayed one clock period in D type flip-flop 47 and coupled back to one of the addend/augend input terminals, (A) of the half adder. Flip-flop 47 is set to a one value at the beginning of each sample period by the signal ST. This insures that a one is added to the LSB of the complemented sample to form the two's complement.

The principles of operation of the FIGURE 6 circuitry may be applied to the circuitry of FIGURE 5 to form a subtracter circuit. This is accomplished by inserting an inverter 33 serially in one of the addend/augend input paths and setting the flip-flop 34 at the beginning of the sample period (rather than resetting the flip-flop as for the adder operations).

FIGURE 7 illustrates an absolute value circuit employing sign-extend registers. The absolute value is formed by two's complementing all samples and applying the samples and their respective complements to a 2:1 multiplexer. The sign bit of the sample being processed conditions the multiplexer to pass the sample if positive, and to pass the two's complement of the sample if negative. In FIGURE 7, the two's complement circuit is designated block 52 and incorporates a combination of elements such as elements 45, 46, 47 and 38 in FIGURE 6. The output of the two's complement block 52 is coupled to one data input terminal of multiplexer 54. The samples, delayed by flip-flop 53 to compensate for the inherent delay in the two's complement circuit 52, are applied to a second data input terminal of multiplexer 54. The output of multiplexer 54 is coupled to registers 55 and 56 which are clocked by CLOCK P. Since the

multiplexer is controlled by the sign bit of the respective sample and since the sign bit occurs after the bits representing the sample value, provision must be made to make the sign bit available at the beginning and throughout the sample period. In the FIGURE 7 arrangement, this is accomplished by tapping the SXSR 50 at the sign bit position, Qs, and storing its value in the "D" type flip-flop 51 under the control of signal ST. The sign bit for a particular sample is applied by flip-flop 51 to the control input of multiplexer 54 for the entire sample period.

FIGURE 8 illustrates a comparator/maximum value circuit which outputs the greater of two samples SA or SB. The two samples SA and SB are serially loaded bit-by-bit into the N-stage registers 66 and 67 respectively, where they are held until the comparison of all the sample bits is completed by comparator 61. The outputs from registers 66 and 67 are coupled to respective data input terminals of multiplexer 68 which is conditioned by the output of comparator 61 to pass the greater of the two samples. A single sign extend latch, 69, is serially coupled to the output of multiplexer 68 in lieu of attaching a sign extend latch to each of the registers 66 and 67.

Comparator 61 operates as follows. Sample SA is serially applied to the non-inverting input of AND gate 60 and to the inverting input of AND gate 62. Sample SB is serially coupled to the inverting input of AND gate 60 and the non-inverting input of AND gate 62. The output terminals of AND gates 60 and 62 are respectively connected to the J and K input terminals of JK flip-flop 63. AND gates 60 and 62 both exhibit logic zero output states if concurrent bits of SA and SB exhibit the same state. AND gate 60 exhibits a logic one output state only when a bit of sample SA is greater than the corresponding bit of sample SB. AND gate 62 exhibits a logic one output state only when a bit of sample SB is greater than the corresponding bit of sample SA. At the beginning of a sample period JK flip-flop 63 is reset so that its output, Q, exhibits a logic zero. When the J and K inputs are 1 and 0 respectively, JK flip-flop 63 will produce a logic one output. Conversely, when the J and K inputs are 0 and 1 respectively, it produces a logic zero output. As samples SA and SB are serially applied to AND gates 60 and 62 and corresponding bits have equal values, both AND gates 60 and 62 exhibit logic zero outputs and JK flip-flop 63 retains the output state determined by the previous (SA, SB) bits. Thus, JK flip-flop 63 outputs a logic zero until AND gate 60 exhibits a logic one. This happens for the first occurrence of SA and SB bits being 1 and 0 respectively at which time the output of JK flip-flop is set to a logic one, indicating that sample SA, at least for the number of bits tested, is greater than

sample SB. The flip-flop retains this state until an occurrence of corresponding bits of SA and SB having 0 and 1 states respectively indicating that sample SB is greater than sample SA. The sample having the most significant logic one, of all of the corresponding unequal pairs of sample bits, determines the output state of flip-flop 63 after all of the value bits of the two samples are serially applied to the comparator.

Provision must be made for polarity differences of two's complement samples since regardless of the value of the value bits, positive numbers are always greater than negative numbers. The condition of SA and SB being of opposite polarity is indicated by the output state of AND gates 60 and 62 when the sample sign bits occur at their inputs. At the occurrence of the sign bits, AND gate 60 exhibits a logic one output state, if sample SA is negative and sample SB is positive. AND gate 62 exhibits a logic one output state if sample SA is positive and sample SB is negative. AND gates 60 and 62 both exhibit logic zeros if samples SA and SB are either both positive or both negative.

It can be shown that for any combination of polarities of samples SA and SB, ORing the output of AND gate 62 with the output of JK flip-flop 63 ANDed with the complement of AND gate 60 will generate a control signal having a logic one state for sample SA greater than sample SB and a logic zero state for sample SB greater than sample SA. In order to generate this control signal, the output of JK flip-flop 63 is coupled to the non-inverting input of AND gate 64 and the output of AND gate 60 is coupled to the inverting input of AND gate 64. The output terminals of AND gates 64 and 62 are coupled to respective input terminals of OR gate 65, the output of which is coupled to the data input terminal of "D" type latch 70. The control signal is loaded into latch 70 after the occurrence of the sign bits and stored for an interval equal to a sample period. The control signal stored in latch 70 is coupled to the control input of multiplexer 68. The control signal may be loaded into latch 70 by the signal XND delayed by, for example, one clock period τ_c . Control signals generated during each sample period are used to control the multiplexer during the subsequent sample period.

FIGURE 1 and FIGURES 3-8 respectively illustrate a sign-extend register for serial digital signal processing and combinations of sign-extend registers with, for example, arithmetic processing devices to form serial digital processing building blocks.

FIGURE 9 is a combination of the aforescribed circuits which form a serial-bit digital detector to provide the envelope of a digital representation of an amplitude modulated carrier. In combining the circuits to form the detector, several of the SXSR

registers are shared by the respective circuits. For illustrative purposes, assume that the signal input to the FIGURE 9 circuit represents a carrier having a frequency of five times the line frequency of a composite NTSC video signal (78.67 KHz) and is modulated by a relatively low frequency signal (less than 20 KHz). Assume also that the signal is a serial-bit two's complement signal occurring at a 300 KHz sample rate. The clock rate is arbitrarily selected to be 10.5 MHz which allows a maximum of 35 clock periods per sample period. Finally, the value of the difference (P-N) between the number of clock pulses of CLOCK P and CLOCK N is chosen to be 11. With the foregoing parameters, the FIGURE 9 circuit may be implemented to detect the presence of the secondary audio program signal (SAP) of the standard Broadcast Television Standards Committee (BSTC) sound signal.

The serial-bit envelope detector incorporates an absolute value circuit 100, similar to the circuit shown in FIGURE 7, a comparator/maximum value circuit, 200, similar to the circuit shown in FIGURE 8 and a subtracter circuit, 300, similar to the circuit of FIGURE 5. Elements in FIGURE 9 are designated with like numerals as their corresponding counterparts in FIGURES 5, 7 and 8. The output register of the absolute value circuit 100 (56 in FIGURE 7) is merged with the comparator register 66. Similarly, the output registers of the subtracter 300 (42 in FIGURE 5) is merged with the comparator register 67.

Input samples X_n are applied to terminal 90 of the absolute value circuit 100. The absolute values of the preceding samples $|X_{n-1}|$, multiplied by two due to the one bit processing delay of elements 52, 53, are output by multiplexer 54 and coupled to the (P-N-1) stage register 55. The added delay of register 55 multiplies the samples from multiplexer 54 by $2^{(P-N-1)}$, thus the samples applied to the input, SA, of comparator/maximum value circuit 200 are equal to $|X_{n-1}| \cdot 2^{(P-N)}$. Since (P-N) was defined as 11 the value of the sample available at input, SA, is $|X_{n-1}|2^{11}$. This sample is coupled to the N-stage register 66 which is clocked by CLOCK P. Clocking a sample into an N-stage register with P clock pulses effects a multiplication by $2^{-(P-N)}$ or 2^{-11} . The sample output from register 66 corresponds to the sample that precedes the sample coupled to its input by one sample period. This sample having undergone a scaling of 2^{11} in register 55 and a scaling of 2^{-11} in register 66 is equal to $|X_{n-2}|$.

The output signal Y_n developed by the comparator/maximum value circuit 200 is the greater of the samples applied to the SA and SB input terminals, delayed by one sample period. Samples Y_n are coupled directly to the subtrahend input terminal, 31, of subtracter 300, and to the minuend input

terminal via the 5-stage register 95. Register 95 multiplies the Y_n samples applied to the minuend input by 2^5 relative to the Y_n samples applied to the subtrahend input. The value output by the full adder 36 is $Y_n(2^5-1)$. This value is coupled to the SB input terminal of comparator/maximum value circuit 200 via flip-flop 38 and register 97 which effect a multiplication of the difference sample by 2^5 . The sample coupled to the SB input terminal is $Y_n(2^5-1) \cdot 2^5$ or $Y_n(1-2^{-5})2^{11}$. Comparator 200 therefore effectively compares the values $|X_{n-1}|$ to the values $Y_n(1-2^{-5})$, and outputs the larger. The factor $(1-2^{-5})$ defines the time constant of the envelope detector. To determine the time constant consider a unit step from one to zero. For the last sample before the step, the output Y_n equals the value one. For the first sample output after the step, the output Y_n equals $(1-2^{-5})$, which is the greater of $Y_n(1-2^{-5})$ and zero. For the n^{th} sample output after the step, the output Y_n equal $(1-2^{-5})^n$. The output decays to $\frac{1}{2}$ after $n=21.8 \approx 22$ output samples. Each sample period equals $1/3000000$ sec. Thus, the time constant of the illustrative circuit is $22/3000000$ or approximately 73 μsec .

In the claims the term sign-extend-register is a clocked shift register having a latch coupled in series at the output of the register to selectively pass sample bits output by the register or to hold a particular bit output by the register under the control of a sign extend signal.

Claims

- Apparatus for processing serial-bit two's complement digital signals whose length may vary occurring in equally spaced intervals with all bits of a sample occurring in less than a sample interval, comprising:
 - a serial arithmetic processing unit (18) having an input and an output terminal;
 - a serial shift register (20) having an input, an output and a clock input terminal; characterized by
 - a sign-extend-register (14,16) having an input, an output, a clock input and a sign-extend signal input terminal and arranging for replicating the sign bit of a sample for the remainder of the sample interval in response to a sign-extend signal;
 - means for serially coupling said serial shift register, said arithmetic processing unit and said sign extend register wherein said arithmetic processing unit is disposed between said registers;
 - means (22) for generating a first clock signal having a first predetermined number of pulses per sample interval (N), a second clock signal having a second predetermined number



registers are shared by the respective circuits. For illustrative purposes, assume that the signal input to the FIGURE 9 circuit represents a carrier having a frequency of five times the line frequency of a composite NTSC video signal (78.67 KHz) and is modulated by a relatively low frequency signal (less than 20 KHz). Assume also that the signal is a serial-bit two's complement signal occurring at a 300 KHz sample rate. The clock rate is arbitrarily selected to be 10.5 MHz which allows a maximum of 35 clock periods per sample period. Finally, the value of the difference (P-N) between the number of clock pulses of CLOCK P and CLOCK N is chosen to be 11. With the foregoing parameters, the FIGURE 9 circuit may be implemented to detect the presence of the secondary audio program signal (SAP) of the standard Broadcast Television Standards Committee (BSTC) sound signal.

The serial-bit envelope detector incorporates an absolute value circuit 100, similar to the circuit shown in FIGURE 7, a comparator/maximum value circuit, 200, similar to the circuit shown in FIGURE 8 and a subtracter circuit, 300, similar to the circuit of FIGURE 5. Elements in FIGURE 9 are designated with like numerals as their corresponding counterparts in FIGURES 5, 7 and 8. The output register of the absolute value circuit 100 (56 in FIGURE 7) is merged with the comparator register 66. Similarly, the output registers of the subtracter 300 (42 in FIGURE 5) is merged with the comparator register 67.

Input samples X_n are applied to terminal 90 of the absolute value circuit 100. The absolute values of the preceding samples $|X_{n-1}|$, multiplied by two due to the one bit processing delay of elements 52, 53, are output by multiplexer 54 and coupled to the (P-N-1) stage register 55. The added delay of register 55 multiplies the samples from multiplexer 54 by $2^{(P-N-1)}$, thus the samples applied to the input, SA, of comparator/maximum value circuit 200 are equal to $|X_{n-1}| \cdot 2^{(P-N)}$. Since (P-N) was defined as 11 the value of the sample available at input, SA, is $|X_{n-1}| \cdot 2^{11}$. This sample is coupled to the N-stage register 66 which is clocked by CLOCK P. Clocking a sample into an N-stage register with P clock pulses effects a multiplication by $2^{-(P-N)}$ or 2^{-11} . The sample output from register 66 corresponds to the sample that precedes the sample coupled to its input by one sample period. This sample having undergone a scaling of 2^{11} in register 55 and a scaling of 2^{-11} in register 66 is equal to $|X_{n-2}|$.

The output signal Y_n developed by the comparator/maximum value circuit 200 is the greater of the samples applied to the SA and SB input terminals, delayed by one sample period. Samples Y_n are coupled directly to the subtrahend input terminal, 31, of subtracter 300, and to the minuend input

terminal via the 5-stage register 95. Register 95 multiplies the Y_n samples applied to the minuend input by 2^5 relative to the Y_n samples applied to the subtrahend input. The value output by the full adder 36 is $Y_n(2^5-1)$. This value is coupled to the SB input terminal of comparator/maximum value circuit 200 via flip-flop 38 and register 97 which effect a multiplication of the difference sample by 2^6 . The sample coupled to the SB input terminal is $Y_n(2^5-1) \cdot 2^6$ or $Y_n(1-2^{-5})2^{11}$. Comparator 200 therefore effectively compares the values $|X_{n-1}|$ to the values $Y_n(1-2^{-5})$, and outputs the larger. The factor $(1-2^{-5})$ defines the time constant of the envelope detector. To determine the time constant consider a unit step from one to zero. For the last sample before the step, the output Y_n equals the value one. For the first sample output after the step, the output Y_n equals $(1-2^{-5})$, which is the greater of $Y_{n-1}(1-2^{-5})$ and zero. For the n^{th} sample output after the step, the output Y_n equal $(1-2^{-5})^n$. The output decays to $\frac{1}{2}$ after $n=21.8 \approx 22$ output samples. Each sample period equals $1/3000000$ sec. Thus, the time constant of the illustrative circuit is $22/3000000$ or approximately 73 μsec .

In the claims the term sign-extend-register is a clocked shift register having a latch coupled in series at the output of the register to selectively pass sample bits output by the register or to hold a particular bit output by the register under the control of a sign extend signal.

Claims

1. Apparatus for processing serial-bit two's complement digital signals whose length may vary occurring in equally spaced intervals with all bits of a sample occurring in less than a sample interval, comprising:

a serial arithmetic processing unit (18) having an input and an output terminal;

a serial shift register (20) having an input, an output and a clock input terminal; characterized by

a sign-extend-register (14,16) having an input, an output, a clock input and a sign-extend signal input terminal and arranging for replicating the sign bit of a sample for the remainder of the sample interval in response to a sign-extend signal;

means for serially coupling said serial shift register, said arithmetic processing unit and said sign extend register wherein said arithmetic processing unit is disposed between said registers;

means (22) for generating a first clock signal having a first predetermined number of pulses per sample interval (N), a second clock signal having a second predetermined number



of pulses per sample interval (P) and said sign-extend signal (XND) occurring at the occurrence of a predetermined sign-bit of said serial-bit digital samples; and

means for coupling said first and second clock signals to the clock input terminals of said serial shift register and sign-extend register respectively, and means for coupling said sign-extend signal to said sign-extend input terminal, whereby as samples are clocked out of the sign extend register the sign-bit of the sample is extended for the remaining pulses of the sample interval.

2. Apparatus according to claim 1, wherein the bits of sample are clocked at a rate of $1/T$, wherein the second predetermined number (P) is greater than the first predetermined number (N), and wherein said sign-extend signal has first and second states and a transition occurring immediately prior to a sign-bit of a serial-bit sample being processed, and wherein P times T is equal to or less than said interval, and said first and second clock signals operate at the same pulse rate $1/T$, and are synchronous.

3. The apparatus as set forth in claim 1 or 2, wherein said serial arithmetic processing unit (SAPU) includes a binary adder comprising:

a full adder circuit (36) having a first addend/augend input terminal coupled to the input terminal of said SAPU, a sum output terminal coupled to the output terminal of said SAPU, having a second addend/augend input terminal for applying a serial-bit sample, a carry-in and a carry-out terminal; and

a one sample bit delay element (34) coupled between said carry-in and said carry-out terminals.

4. The apparatus set forth in claim 3 further including an inverter (33) interposed between the input terminal of the SAPU and said first addend/augend input terminal; and

means (SET) to set said delay element to a one state at the beginning of each sample period wherein said full adder provides the difference between serial samples applied to its second and first addend/augend input terminals.

5. The apparatus set forth in claim 1 or 2 wherein said serial arithmetic processing unit (SAPU) includes a two's complementing circuit comprising:

an inverter (45) serially coupled to the input terminal of said SAPU;

a half-adder (46) having a first addend/augend input terminal serially coupled to said inverter, a second addend/augend input terminal, a sum output terminal coupled to the output terminal of said SAPU and a carry-out output terminal;

a one sample bit period delay element (47) coupled between said carry-out output terminal and the second addend/augend input terminal; and

means (SET) for setting said delay element to a one state at the beginning of each sample interval.

6. The apparatus set forth in claim 1 or 2 wherein the serial arithmetic processing unit (SAPU) includes a binary multiplier for multiplying serial-bit samples by 2^K , where K is an integer, comprising a K-stage shift register (26) coupled between the input and output terminals of said SAPU.

7. The apparatus set forth in claim 1 or 2 wherein said serial arithmetic processing unit (SAPU) includes an absolute value circuit (51,52,53,54,55) and the register (50) coupled to the input terminal of the SAPU includes a tap for providing a sign-bit of said two's complement samples at the beginning of each sample period, said absolute value circuit comprising:

a latch (51) coupled to said tap for storing said sign bit;

switch means (54) having an output terminal coupled to the output terminal of the SAPU, first and second data input terminals, and having a control terminal coupled to said latch, for alternatively applying samples applied to said first and second data input terminals for said sign-bit being a one or zero respectively;

a serial-bit two's complement circuit (52) having an input terminal coupled to the input terminal of the SAPU, and an output terminal coupled to said first data input terminal;

a compensating delay element (53) coupled between the input terminal of said SAPU and the second data input terminal, said compensating delay element providing a delay period equivalent to the processing delay of said two's complement circuit.

8. The apparatus set forth in claim 7 wherein the shift register (output register) coupled to the output terminal of the SAPU is merged into comparing means comprising:

a first input terminal coupled to a predetermined stage of the output register (66), the number of stages between said predetermined



stage and the output of said register being N in number where N is an integer, and a second input terminal for applying a serial-bit sample to be compared with samples applied to said first input terminal;

an N-stage shift register (67) having an input terminal coupled to said second input terminal, and having an output terminal;

further switch means (68) having first and second data input terminals coupled respectively to the output terminals of said output register and said N-stage register, a control input terminal, and an output terminal at which the greater of the samples applied to the first and second input terminals is produced;

means (60,62,63,64,65) coupled to the first and second input terminals for producing a control signal exhibiting a first output state if the sample applied to the first input terminal exhibits a logic one in a more significant bit position, excluding sign bits, than the sample applied to the second input terminal, or the sample applied to the first input terminal is positive and the sample applied to the second input terminal is negative, and exhibits a second state otherwise; and

a latch (70) for coupling said control signal to said further switch means, wherein said further switch means couples said output register or the N-stage register to its output terminal for the control signal exhibiting first and second states respectively.

9. The apparatus set forth in claim 8 wherein said means for producing a control signal comprises:

first (60) and second (62) AND gates having respective non-inverting inputs coupled to said first and second input terminals respectively and having respective inverting inputs coupled to said second and first input terminals respectively and having respective output terminals;

a JK flip-flop (63) having J and K input terminals respectively coupled to the output terminals of said first and second AND gates, respectively and having an output terminal;

a third AND gate (64) having inverting and non-inverting input terminals coupled to the output terminals of said first AND gate and said JK flip-flop respectively, and having an output terminal; and

an OR gate (65) having respective input terminals coupled to the output terminals of said third and second AND gates and an output terminal coupled to said latch.

Patentansprüche

1. Einrichtung zum Verarbeiten bitserieller Zweierkomplement-Digitalsignale, deren Länge sich ändern kann und die in gleich beabstandeten Intervallen auftreten, wobei alle Bits eines Abtastwertes (Sample) in weniger als einem Abtastintervall liegen, enthaltend:

- eine Seriell-Arithmetik-Verarbeitungseinheit (18) mit einem Eingangs- und einem Ausgangsanschluß;
- ein Seriell-Schieberegister (20) mit einem Eingangs-, einem Ausgangs- und einem Takteingangs-Anschluß; gekennzeichnet durch
- ein Vorzeichen-Erweiterungsregister (14,16) mit einem Eingang, einem Ausgang, einem Takteingang und einem Vorzeichenerweiterungs-Signal-Eingangsanschluß, das so aufgebaut ist, daß das Vorzeichenbit eines Abtastwertes für den Rest des Abtast-Intervalls ansprechend auf ein Vorzeichen-Erweiterungssignal wiederholt wird;
- Mittel zum seriellen Koppeln des Seriell-Schieberegisters, der Arithmetik-Verarbeitungseinheit und des Vorzeichen-Erweiterungsregisters, wobei zwischen den Registern die Arithmetik-Verarbeitungseinheit angeordnet ist;
- Mittel (22) zum Erzeugen eines ersten Taktsignals mit einer ersten vorbestimmten Zahl von Impulsen pro Abtast-Intervall (N), einem zweiten Taktsignal mit einer zweiten vorbestimmten Anzahl von Impulsen pro Abtastintervall (P), wobei das Vorzeichen-Erweiterungssignal (XND) beim Auftreten eines vorbestimmten Vorzeichenbits der Digital-Abtastwerte mit seriellen Bits auftritt;
- Mittel zum Koppeln des ersten und des zweiten Taktsignals an den Takt-Eingangsanschluß des Seriell-Schieberegisters bzw. Vorzeichen-Erweiterungsregisters und Mittel zum Koppeln des Vorzeichen-Erweiterungssignals an den Vorzeichen-Erweiterungs-Eingangsanschluß, wobei beim Heraustakten von Abtastwerten aus dem Vorzeichen-Erweiterungsregister das Vorzeichenbit des Abtastwertes für die verbleibenden Impulse des Abtast-Intervalls verlängert/erweitert wird.

2. Einrichtung nach Anspruch 1, bei der die Bits des Abtastwertes mit einer Frequenz $1/T$ getaktet werden, wobei die zweite vorbestimmte Zahl (P) größer als die erste vorbestimmte Zahl (N) ist und wobei das Vorzeichen-Erweite-



rungssignal erste und zweite Zustände und einen Übergang hat, der unmittelbar vor einem verarbeiteten Vorzeichenbit eines Bitseriell-Abtastwertes auftritt, und wobei P mal T gleich oder kleiner als das Intervall ist und die ersten und zweiten Taktsignale mit denselben Impuls-Raten $1/T$ arbeiten und synchron sind.

3. Einrichtung nach Anspruch 1 oder 2, bei der die Seriell-Arithmetik-Verarbeitungseinheit (SAPU; serial arithmetic processing unit) einen Binär-Addierer enthält, mit:

- einer Volladdierer-Schaltung (36) mit einem ersten Addend/Augend-Eingangsanschluß, der mit dem Eingangsanschluß der SAPU gekoppelt ist, einem Summen-Ausgangsanschluß, der mit dem Ausgangsanschluß der SAPU gekoppelt ist, mit einem zweiten Addend/Augend-Eingangsanschluß zum Anlegen eines Bitseriell-Abtastwertes, einem Übertrags-Eingangs- und einem Übertrags-Ausgangsanschluß; und
- einem um ein Abtastwert-Bit verzögern- den Verzögerungs-Element (34), das zwischen Übertrags-Eingangs- und Übertrags-Ausgangs-Anschluß gekoppelt ist.

4. Einrichtung nach Anspruch 3, weiter beinhaltend:

- einen Inverter (33), der zwischen dem Eingangs-Anschluß der SAPU und dem ersten Addend/Augend-Eingangsanschluß eingefügt ist;
- Mittel (SET) zum Setzen/Voreinstellen des Verzögerungs-Elementes auf einen Zustand am Anfang jeder Abtast-Periode, wobei der Volladdierer die Differenz zwischen Seriell-Abtastwerten bildet, die an seinen zweiten und ersten Addend/Augend-Eingangsanschluß angelegt sind.

5. Einrichtung nach einem der Ansprüche 1 oder 2, bei der die Seriell-Arithmetik-Verarbeitungseinheit (SAPU) eine Zweier-Komplementschaltung beinhaltet, die enthält:

- einen mit dem Eingangsanschluß der SAPU seriell gekoppelten Inverter (45);
- einen Halbaddierer (46) mit einem ersten und einem zweiten Addend/Augend-Eingangsanschluß, der mit dem Inverter in Serie geschaltet ist, einem zweiten Addend/Augend-Eingangsanschluß, einem mit dem Ausgangsanschluß der SAPU gekoppelten Summen-Ausgangsanschluß und einem Ausgangs-Übertrag-Ausgangsanschluß;

- ein um eine Abtastbit-Periode verzögern- des Element (47), das zwischen den Ausgangs-Übertrags-Ausgangsanschluß und den zweiten Addend/Augend-Eingangsanschluß gekoppelt ist; und
- Mittel (SET) zum Setzen/Voreinstellen des Verzögerungselementes auf einen Eins-Zustand am Anfang jedes Abtast-Intervalls.

6. Einrichtung nach Anspruch 1 oder 2 bei der die Seriell-Arithmetik-Verarbeitungseinheit (SAPU) einen Binär-Multiplizierer zum Multiplizieren bitserieller Abtastwerte mit 2^K enthält, wobei K eine ganze Zahl ist, der ein K-stufiges Schieberegister (26) enthält, das zwischen den Eingangs- und Ausgangs-Anschluß der SAPU gekoppelt ist.

7. Einrichtung nach Anspruch 1 oder 2, bei der die Seriell-Arithmetik-Verarbeitungseinheit (SAPU) eine Absolutwert-Schaltung (51 bis 55) beinhaltet und das an den Eingangsanschluß der SAPU gekoppelte Register (50) eine Anzapfung enthält zum Abgeben eines Vorzeichenbits der Zweierkomplement-Abtastwerte am Anfang jeder Abtastwert-Periode, wobei die Absolutwert-Schaltung aufweist:

- ein Latch (51), das zum Speichern des Vorzeichen-Bits mit der Anzapfung gekoppelt ist;
- Schaltmittel (54) mit einem an den Ausgangsanschluß der SAPU gekoppelten Ausgangsanschluß, mit ersten und zweiten Daten-Eingangsanschlüssen und mit einem Steueranschluß, der mit dem Latch zum alternativen Anlegen von Abtastwerten gekoppelt ist, die an den ersten und zweiten Daten-Eingangsanschluß angelegt werden, wenn das Vorzeichen-Bit eine Eins bzw. Null ist;
- eine Seriell-Bit-Zweierkomplement-Schaltung (52) mit einem an den Eingangsanschluß der SAPU gekoppelten Eingangsanschluß und mit einem an den ersten Daten-Eingangsanschluß gekoppelten Ausgangsanschluß;
- ein Kompensations-Verzögerungselement (53), das zwischen den Eingangsanschluß der SAPU und den zweiten Daten-Eingangsanschluß gekoppelt ist und das eine Verzögerungszeit bewirkt, die der Verarbeitungszeit der Zweier-Komplement-Schaltung entspricht.

8. Einrichtung nach Anspruch 7, bei der das mit dem Ausgangs-Anschluß der SAPU gekoppelte Schieberegister (Ausgangs-Register) in dem



Vergleichermittel enthalten ist, beinhaltend:

- einen ersten Eingangs-Anschluß, der mit einer vorbestimmten Stufe des Ausgangsregisters (66) gekoppelt ist, wobei die Anzahl der Stufen zwischen der vorbestimmten Stufe und dem Ausgang des Registers N beträgt, wobei N eine ganze Zahl ist, und einen zweiten Eingangsanschluß zum Anlegen eines Bitseriell-Abtastwertes, der mit den an den ersten Eingangsanschluß angelegten Abtastwerten zu vergleichen ist; 5
- ein N-stufiges Schieberegister (67) mit einem an den zweiten Eingangsanschluß gekoppelten Eingangsanschluß und mit einem Ausgangs-Anschluß; 10
- weiteres Schaltmittel (68) mit ersten und zweiten Daten-Eingangs-Anschlüssen, die jeweils an die Ausgangsanschlüsse des Ausgangs-Registers bzw. des N-stufigen Registers gekoppelt sind, mit einem Steuer-Eingangsanschluß und mit einem Ausgangs-Anschluß, an dem der größere der an die ersten und zweiten Eingangsanschlüsse angelegten Abtastwerte abgegeben wird; 15
- Mittel (60,62,63,64,65), das mit dem ersten und zweiten Eingangsanschluß gekoppelt ist, zum Erzeugen eines Steuersignals, das einen ersten Ausgangs-Zustand aufweist, wenn der an den ersten Eingangsanschluß angelegte Abtastwert eine logische Eins in einer signifikanteren Bitposition enthält, mit Ausnahme der Vorzeichenbits, als der an den zweiten Eingangsanschluß angelegte Abtastwert oder der an den ersten Eingangsanschluß angelegte Abtastwert positiv ist und der an dem zweiten Eingangsanschluß angelegte Abtastwert negativ ist und anderenfalls einen zweiten Zustand aufweist; und 20
- ein Latch (70) zum Koppeln des Steuersignals an das weitere Schaltmittel, wobei das weitere Schaltmittel das Ausgangs-Register oder das N-stufige Register an seinen Ausgangsanschluß koppelt, wenn das Steuersignal den ersten bzw. zweiten Zustand aufweist. 25

9. Einrichtung nach Anspruch 8, bei der das Mittel zum Erzeugen eines Steuersignals enthält:

- erstes (60) und zweites (62) UND-Gater mit jeweiligem nicht-invertierenden Eingang, die an den ersten bzw. zweiten Eingangsanschluß gekoppelt sind und mit jeweiligem invertierenden Eingang, die an den zweiten bzw. ersten Ein-

gangsanschluß angelegt sind und mit einem jeweiligen Ausgangs-Anschluß;

- ein JK-Flipflop (63) mit J- und K-Eingangsanschluß, die an den Ausgangs-Anschluß des ersten bzw. zweiten UND-Gaters gekoppelt sind, und mit einem Ausgangs-Anschluß;
- ein drittes UND-Gater (64) mit einem invertierenden und nicht-invertierenden Eingangsanschluß, die an die Ausgangsanschlüsse des ersten UND-Gaters bzw. das JK-Flipflop gekoppelt sind, und mit einem Ausgangsanschluß;
- ein ODER-Gater (65) mit jeweils an den Ausgangs-Anschluß des dritten bzw. zweiten UND-Gaters gekoppelten Eingangs-Anschlüssen und mit einem an das Latch gekoppelten Ausgangs-Anschluß.

Revendications

1. Dispositif pour traiter des signaux numériques de complément à deux de binaires sériels dont la longueur peut varier, se produisant selon des intervalles également espacés, l'ensemble des bits d'un échantillon occupant des intervalles inférieurs à un intervalle d'échantillonnage, comprenant :

une unité de traitement arithmétique sériel (18) comportant une borne d'entrée et une borne de sortie ;

un registre à décalage sériel (20) comportant une borne d'entrée, une borne de sortie et une borne d'entrée d'horloge, caractérise par :

un registre d'extension de signe (14,16) comportant une borne d'entrée, une borne de sortie, une borne d'entrée d'horloge et une borne d'entrée d'un signal d'extension de signe et étant disposé pour répéter le binaire de signe d'un échantillon pour le reste de l'intervalle d'échantillonnage en réponse à un signal d'extension de signe ;

un moyen pour coupler en série ledit registre à décalage sériel, ladite unité de traitement arithmétique et ledit registre d'extension de signe dans lequel ladite unité de traitement arithmétique est disposée entre lesdits registres ;

un moyen (22) pour produire un premier signal d'horloge comportant un premier nombre prédéterminé d'impulsions par intervalle d'échantillonnage (N), un second signal d'horloge comportant un second nombre prédéterminé d'impulsions par intervalle d'échantillonnage (P) et ledit signal d'extension de signe (XND) se produisant à l'occurrence d'un binaire



de signe prédéterminé desdits échantillons numériques de binaires sériels ; et

un moyen pour coupler lesdites premier et second signaux d'horloge respectivement aux bornes d'entrée d'horloge dudit registre à décalage sériel et dudit registre d'extension de signe et un moyen pour coupler ledit signal d'extension de signe à ladite borne d'entrée du signal d'extension de signe , de sorte que, comme les échantillons sont pointés en sortie du registre d'extension de signe , le binaire de signe de l'échantillon est étendu aux impulsions restantes de l'intervalle d'échantillonnage.

2. Dispositif selon la revendication 1 dans lequel les binaires d'un échantillon sont rythmés à une fréquence de $1/T$, dans lequel le second nombre prédéterminé (P) est supérieur au premier nombre prédéterminé (N) et dans lequel ledit signal d'extension de signe comporte un premier et un second état et une transition se produisant immédiatement avant un bit de signe d'un échantillon de binaires sériels à traiter et dans lequel P fois T est égal ou inférieur audit intervalle et lesdits premier et second signaux d'horloge fonctionnent à la même fréquence d'impulsions $1/T$ et sont synchrones.

3. Dispositif selon la revendication 1 ou 2 dans lequel ladite unité de traitement arithmétique sériel (SAPU) inclut un additionneur binaire comprenant:

un circuit additionneur (36) comportant une première borne d'entrée cumulateur/cumulande couplée à la borne d'entrée de ladite SAPU, une borne de sortie de la somme couplée à la borne de sortie de ladite SAPU, comportant une seconde borne d'entrée cumulateur/cumulande pour appliquer un échantillon de binaires sériels, une borne de report en entrée et une borne de report de sortie ; et

un élément à retard d'un bit d'échantillon (34) couplé entre lesdites bornes de port d'entrée et de port de sortie.

4. Dispositif selon la revendication 3 comprenant , de plus, un inverseur (33) interposé entre la borne d'entrée de la SAPU et ladite première borne d'entrée cumulateur/cumulande ; et

un moyen (SET) pour établir ledit élément à retard dans un premier état au début de chaque période d'échantillonnage dans lequel ledit additionneur fournit la différence entre les échantillons sériels appliqués à ses seconde et première bornes d'entrée cumulateur/cumulande.

5. Dispositif selon la revendication 1 ou 2 , dans lequel ladite unité de traitement arithmétique sériel (SAPU) inclut un circuit de complément à deux, comprenant :

un inverseur (45) couplé en série à la borne d'entrée de ladite SAPU ;

un demi-additionneur (46) comportant une première borne d'entrée cumulateur/cumulande couplée en série audit inverseur, une seconde borne d'entrée cumulateur/cumulande, une borne de sortie de la somme couplée à la borne de sortie de ladite SAPU et une borne de report en sortie ;

un élément à retard d'une période d'un bit d'échantillon (47) couplé entre ladite borne de report en série et la seconde borne d'entrée cumulateur/cumulande ; et

un moyen (SET) pour établir ledit élément à retard dans un premier état au début de chaque intervalle d'échantillonnage.

6. Dispositif selon la revendication 1 ou 2, dans lequel l'unité de traitement arithmétique sériel (SAPU) comprend un multiplicateur binaire pour multiplier les échantillons de binaires en série par 2^K , où K est un entier, comprenant un registre à décalage à K étapes (26) couplé entre les bornes d'entrée et de sortie de ladite SAPU.

7. Dispositif selon la revendication 1 ou 2, dans lequel ladite unité de traitement arithmétique sériel (SAPU) comprend un circuit de valeur absolue (51, 52, 53, 54, 55) et le registre (50) couplé à la borne d'entrée de la SAPU inclut une connexion pour maintenir un binaire de signe desdits échantillons de complément à deux au début de chaque période d'échantillonnage, ledit circuit de valeur absolue comprenant :

une bascule (51) couplée à ladite connexion pour enregistrer ledit binaire de signe ;

un moyen de commutation (54) comportant une borne de sortie couplée à la borne de sortie de la SAPU, une première et une seconde bornes d'entrée de données, et comportant une borne de commande couplée à ladite bascule pour appliquer alternativement les échantillons appliqués auxdites première et seconde bornes d'entrée de données afin que ledit binaire de signe soit respectivement un un ou un zéro ;

un circuit de complément à deux de binaires sériels (52) comportant une borne d'entrée couplée à la borne d'entrée de la SAPU, et une borne de sortie couplée à ladite première borne d'entrée de données ;



un élément à retard de compensation (53) couplé entre la borne d'entrée de ladite SAPU et la seconde borne d'entrée de données, ledit élément à retard de compensation fournissant une période de retard équivalente au retard de traitement dudit circuit de complément à deux.

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8. Dispositif selon la revendication 7, dans lequel le registre à décalage (registre de sortie) couplé à la borne de sortie de la SAPU est fusionné aux moyens de comparaison comprenant :

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une première borne d'entrée couplée à une étape prédéterminée du registre de sortie (66), le nombre d'étapes entre ladite étape prédéterminée et la sortie dudit registre étant N en nombre où N est un entier, et une seconde borne d'entrée pour appliquer un échantillon de binaires sériels à comparer avec des échantillons appliqués à ladite première borne d'entrée;

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un registre à décalage à N étapes (67) comportant une borne d'entrée couplée à ladite seconde borne d'entrée et comportant une borne de sortie ;

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un autre moyen de commutation (68) comportant des premières et secondes bornes d'entrée de données couplées respectivement aux bornes de sortie dudit registre de sortie et dudit registre à N étapes, une borne d'entrée de commande, et une borne de sortie au niveau de laquelle est produit le plus grand des échantillons appliqués aux première et seconde bornes d'entrée ;

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des moyens (60, 62, 63, 64, 65) couplés aux première et seconde bornes d'entrée pour produire un signal de commande présentant un premier état de sortie si l'échantillon appliqué à la première borne d'entrée présente un un logique dans une position de bit plus significatif, excluant les bits de signe, que l'échantillon appliqué à la seconde borne d'entrée, ou si l'échantillon appliqué à la première borne d'entrée est positif et l'échantillon appliqué à la seconde borne d'entrée est négatif, et présente autrement un second état ; et

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une bascule (70) pour coupler ledit signal de commande audit moyen de commutation supplémentaire, dans lequel ledit moyen de commutation supplémentaire couple ledit registre de sortie ou le registre à N étapes à sa borne de sortie pour que le signal de commande présente respectivement des premier et second états.

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9. Dispositif selon la revendication 8 dans lequel lesdits moyens pour produire un signal de commande comprennent :

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une première (60) et une seconde (62)

portes ET comportant des entrées respectives non inverseuses couplées auxdites première et seconde bornes d'entrée, respectivement, et comportant des entrées respectives inverseuses couplées auxdites seconde et première bornes d'entrée respectivement, et comportant des bornes de sortie respectives ;

une bascule JK (63) comportant des bornes d'entrée J et K respectivement couplées aux bornes de sortie desdites première et seconde portes ET, respectivement et comportant une borne de sortie ;

une troisième porte ET (64) comportant des bornes d'entrée inverseuse et non inverseuse couplées aux bornes de sortie de ladite première porte ET et de ladite bascule JK, respectivement, et comportant une borne de sortie ; et

une porte OU (65) comportant des bornes d'entrée respectives couplées aux bornes de sortie desdites troisième et seconde portes ET et une borne de sortie couplée à ladite bascule.