CLAIMS

1. An enhancement mode switching device, comprising:

a substrate;

a nitride transistor structure arranged on the substrate;

a dielectric layer formed on the nitride transistor structure, wherein a gate region and two ohmic contact regions respectively located at two sides of the gate region are defined on the dielectric layer, and each of the two ohmic contact regions is through the dielectric layer;

a groove formed in the gate region ~~and at least partially through the dielectric layer~~;

p-type semiconductor material formed in the groove; and

a source electrode and a drain electrode located at the two ohmic contact regions,

wherein, the groove is partially through the dielectric layer and the p-type semiconductor material directly contacts the dielectric layer at the bottom of the groove, or

wherein, the groove is completely through the dielectric layer and the device comprises further an additional dielectric layer formed in the groove under the p-type semiconductor material.

2. The enhancement mode switching device according to claim 1, wherein the nitride transistor structure comprises:

a nitride nucleation layer located on the substrate;

a nitride buffer layer located on the nitride nucleation layer; and

a nitride channel layer located on the nitride buffer layer.

3. The enhancement mode switching device according to claim 2, wherein the nitride channel layer is non-doped or n-type doped.

4. The enhancement mode switching device according to claim 2, wherein the nitride transistor structure further comprises a nitride barrier layer arranged on the nitride channel layer.

5. The enhancement mode switching device according to claim 4, wherein the nitride transistor structure further comprises a nitride cap layer formed on the nitride

barrier layer.

6. The enhancement mode switching device according to claim 5, wherein nitride in the nitride cap layer is gallium nitride or aluminum gallium nitride.

7. The enhancement mode switching device according to claim 1, wherein the dielectric layer comprises a silicon nitride layer, ~~and/~~or a silicon dioxide layer, ~~and/~~or an aluminum nitride layer, ~~and/~~or an aluminum silicon nitride layer, ~~and/~~or an aluminum oxide layer, ~~and/~~or an aluminum oxynitride layer, ~~and/~~or hafnium oxide, ~~and/~~or silicon oxynitride, ~~and/~~or hafnium aluminum oxide.

8. The enhancement mode switching device according to claim 1, wherein the p-type semiconductor material is selected from p-type diamond, p-type NiO, p-type GaN or p-type polycrystalline GaN.

9. The enhancement mode switching device according to claim 1, further comprising a conductive metal layer formed on the p-type semiconductor material.

~~10. The enhancement mode switching device according to claim 1, wherein an additional dielectric layer is further deposited on an inner wall of the groove, and the p-type semiconductor material is formed on the additional dielectric layer.~~

~~11~~10. The enhancement mode switching device according to claim ~~10~~1, wherein material of the additional dielectric layer is selected from one or any combination of Al_2O_3, AlON, SiN, SiON, SiO_2 and HfO_2.

~~12~~11. A method for fabricating an enhancement mode switching device, comprising steps as follows:

providing a substrate, and forming a nitride transistor structure on the substrate;

forming a dielectric layer on the nitride transistor structure, wherein a gate region is defined on the dielectric layer;

forming, in the gate region, a groove extending toward the nitride transistor structure~~, wherein the groove is at least partially through the dielectric layer~~;

forming p-type semiconductor material in the groove;

etching the dielectric layer except for the gate region in the dielectric layer to form two ohmic contact regions; and

forming a source electrode and a drain electrode at the two ohmic contact regions, respectively,

wherein, the groove is partially through the dielectric layer and the p-type

semiconductor material directly contacts the dielectric layer at the bottom of the groove, or

wherein, the groove is completely through the dielectric layer, and the method comprises further forming an additional dielectric layer in the groove, and the step of forming p-type semiconductor material in the groove comprises forming the p-type semiconductor material on the additional dielectric layer in the groove.

~~13~~12. The method for fabricating the enhancement mode switching device according to claim ~~12~~11, further comprising forming a conductive metal layer on the p-type semiconductor material after forming the p-type semiconductor material in the groove.

~~14~~13. The method for fabricating the enhancement mode switching device according to claim ~~12~~11, wherein the step of forming the nitride transistor comprises:

forming a nitride nucleation layer on the substrate;

forming a nitride buffer layer on the nitride nucleation layer; and

forming a nitride channel layer on the nitride buffer layer, wherein the nitride channel layer is non-doped or n-type doped; and

forming a nitride barrier layer on the nitride channel layer.

~~15~~14. The method for fabricating the enhancement mode switching device according to claim ~~14~~13, further comprising forming a nitride cap layer on the nitride barrier layer, wherein nitride in the nitride cap layer is gallium nitride or aluminum gallium nitride.

~~16~~15. The method for fabricating the enhancement mode switching device according to claim ~~12~~11, wherein the dielectric layer comprises a silicon nitride layer, ~~and/~~or a silicon dioxide layer, ~~and/~~or an aluminum nitride layer, ~~and/~~or an aluminum silicon nitride layer, ~~and/~~or an aluminum oxide layer, ~~and/~~or an aluminum oxynitride layer, ~~and/~~or hafnium oxide, ~~and/~~or silicon oxynitride, ~~and/~~or hafnium aluminum oxide.

~~17~~16. The method for fabricating the enhancement mode switching device according to claim ~~12~~11, ~~further comprising~~wherein forming an additional dielectric layer in the groove comprises performing oxidation treatment on the dielectric layer ~~before forming the p-type semiconductor material in the groove~~.

~~18~~17. The method for fabricating the enhancement mode switching device according to claim ~~12~~11, ~~further comprising~~wherein forming an additional dielectric layer in the groove comprises depositing ~~an~~ the additional dielectric layer on an inner

wall of the groove ~~before forming the p-type semiconductor material in the groove~~.

~~19~~18. The method for fabricating the enhancement mode switching device according to claim ~~18~~11, wherein material of the additional dielectric layer is selected from one or any combination of Al_2O_3, AlON, SiN, SiON, SiO_2 and HfO_2.