CLAIMS:

1. A method for manufacturing a semiconductor substrate, said method comprising:

forming a patterned first conductor trace layer on a sacrificial carrier, wherein the patterned first conductor trace layer comprises a plurality of conductor layouts, and wherein the patterned first conductor trace layer is formed by coating a surface of the sacrificial carrier with a photoresist, exposing the photoresist with a mask, selectively etching away the photoresist, obtaining a patterned photoresist, depositing a first electric conductor material into the patterned photoresist, and removing the photoresist to form the patterned first conductor trace layer;

forming a first interconnect layer on the patterned first conductor trace layer, wherein the first interconnect layer comprises conductor interconnect studs that connect with selected areas of the patterned first conductor trace layer;

disposing the patterned first conductor trace layer and the first interconnect layer in a mold cavity with the sacrificial carrier defining one side of the mold cavity, and encapsulating the patterned first conductor trace layer and the first interconnect layer in the mold cavity with a molding compound comprising a matrix of resin and silica fillers, heating the molding compound to its molten form and densely packing under pressure into the patterned first conductor trace layer and the first interconnect layer to form a first insulator layer and the molding compound-conductor interfaces in the first conductor trace layer and the first interconnect layer become liquid impenetrable;

curing the molding compound to form a first molded encapsulation; and

abrasively grinding a free surface of the first molded encapsulation to expose both the conductor interconnect studs and the silica fillers on the ground surface, so that the ground surface is planar with the sacrificial carrier.

2. The manufacturing method according to claim 1, further comprising:

forming a patterned second conductor trace layer which connects with selected conductors at the first interconnect layer;

forming a second interconnect layer comprising conductor interconnect studs that connect with selected areas on the patterned second conductor trace layer;

disposing the second patterned conductor trace layer and the second interconnect layer in a mold cavity with the sacrificial carrier or the ground surface of the first molded encapsulation defining one side of the mold cavity, and encapsulating the second

patterned conductor trace layer and the second interconnect layer in the mold cavity with a molding compound comprising a matrix of resin and silica fillers, thereby, when the molding compound is molten, it is densely packed under pressure to encapsulate the patterned second conductor trace layer and the second interconnect layer and the molding compound-conductor interfaces in the second conductor trace layer and the second interconnect layer become liquid impenetrable;

curing the molding compound to form a second molded encapsulation on top of the first molded encapsulation; and

abrasively grinding a free surface of the second molded encapsulation to expose both the second conductor interconnect studs and the silica fillers on the ground surface, so that the ground surface is planar with the sacrificial carrier.

3. The manufacturing method according to claim 2, further comprising:

repeating the above steps of forming, disposing and abrasively grinding to build up three or more layers of the semiconductor substrate.

4. The manufacturing method according to claim 3, wherein abrasively grinding the molded encapsulation comprises exposing the silica fillers to promote adhesion of the next contiguous layer.

5. The manufacturing method according to claim 1 or 2, wherein abrasively grinding the molded encapsulation comprises displacing the exposed silica fillers away on the ground surface of the molded encapsulation to create a dimpled surface to promote adhesion of the next contiguous layer.

6. The manufacturing method according to claim 1 or 2, further comprising depositing an adhesion layer on the ground surface of the molded encapsulation.

7. The manufacturing method according to claim 6, wherein depositing the adhesion layer comprises depositing a polyimide layer or a photo-imageable layer.

8. The manufacturing method according to claim 3, further comprising:

forming an adhesion layer on the last ground dimpled surface;

forming an outermost conductor trace layer on the adhesion layer;

sealing the outermost conductor trace layer with a soldermask layer; and

selectively exposing areas of the outermost conductor trace layer for external electrical connection.

9. The manufacturing method according to any one of claims 2-8, wherein, when the sacrificial carrier forms one side of the mold cavity and the mold cavity is larger than the first encapsulation or subsequent encapsulation, the new encapsulation becomes an overmolding over the first or subsequent encapsulation.

10. The manufacturing method according to claim 8, further comprising:

removing an internal portion of the sacrificial carrier to expose the first conductor trace layer, thereby leaving a reinforcement carrier ring around a periphery of the semiconductor substrate or selectively removing internal portions of the sacrificial carrier to expose a gang of the first conductor trace layer, thereby leaving reinforcement carrier rings around conductor trace layouts located in the first conductor trace layer.

11. A semiconductor substrate comprising a single or multiple layered molded encapsulation obtained directly from the manufacturing method defined by claims 1-10 wherein the first conductor trace layer and the outermost conductor trace layer are separately exposed for external electrical connections.

12. A method of manufacturing a semiconductor substrate comprising:

preparing a sacrificial carrier with two substantially parallel faces;

forming a patterned first conductor trace layer on one face of the sacrificial carrier, wherein the patterned first conductor trace layer comprises a plurality of patterned conductor layouts, and wherein the patterned first conductor trace layer is formed by coating the one surface of the sacrificial carrier with a photoresist, exposing the photoresist with a mask, selectively etching away the photoresist, obtaining a patterned photoresist, depositing a first electric conductor material into the patterned photoresist, and removing the photoresist to form the patterned first conductor trace layer;

forming a first interconnect layer on the patterned first conductor trace layer, with the first interconnect layer comprising conductor interconnect studs that connect with selected areas on the patterned first conductor trace layer;

disposing the patterned first conductor trace layer and the first interconnect layer in a mold cavity, introducing a molding compound comprises a matrix of resin and silica fillers in its molten form into the mold cavity and allowing the molding compound to cure and form a first insulator layer, thereby the molding compound is densely packed under pressure to encapsulate the patterned first conductor trace layer and the first interconnect layer and the molding compound-conductor interfaces in the first conductor trace layer and the first interconnect layer become liquid impenetrable; and

removing a depth of the first insulator layer by abrasively grinding a surface of the first insulator layer to expose both the conductor interconnect studs and the silica fillers on the ground surface, so that the ground surface is planar with the sacrificial carrier.

13. The manufacturing method according to claim 12, further comprising forming a plurality of peripheral conductors around and isolated from the patterned conductor layouts of the patterned first conductor trace layer.

14. The manufacturing method according to claim 12, wherein the first insulator layer is formed by densely packing the molten molding compound by injection or compression molding.

15. The manufacturing method according to claim 12, wherein the step of forming the first insulator layer comprising:

disposing the sacrificial carrier with the patterned first conductor trace layer and the first interconnect layer formed thereon in one or more mold cavities;

densely packing the molten molding compound into the patterned first conductor trace layer and the first interconnect layer in the mold cavity or mold cavities so that conductor-molding compound interfaces are liquid impenetrable; and

solidifying the molding compound to form a compact composite structure with the patterned first conductor trace layer and the first interconnect layer.

16. The manufacturing method according to claim 15, wherein the sacrificial carrier with the patterned first conductor trace layer and the first interconnect layer formed thereon is disposed in a plurality of mold cavities to form a gang of insulator layers on the sacrificial carrier.

17. The manufacturing method according to claim 12, wherein the abrasive grinding exposes the silica fillers and forms a plurality of dimples on the ground surface.

18. The manufacturing method according to claim 17, wherein after the step of removing a depth of the first insulator layer, the manufacturing method further comprises depositing an adhesion layer on the ground surface, wherein the adhesion layer covers the plurality of dimples to form a planar surface.

19. The manufacturing method according to claim 12, further comprising:

forming a patterned second conductor trace layer on the first insulator layer; and

sealing the patterned second conductor trace layer with a second insulator layer and exposing selected areas of the patterned second conductor trace layer through the second insulator layer for external electric connection.

20. The manufacturing method according to claim 19, further forming additional build-up layers which comprises:

forming a patterned third conductor trace layer on the second insulator layer; and

repeating the above steps of forming an interconnect layer, forming an insulator layer and removing a depth of the insulator layer by abrasive grinding.

21. The manufacturing method according to claim 12, further comprising:

forming a patterned second conductor trace layer on the first insulator layer;

forming a second interconnect layer on the patterned second conductor trace layer;

forming a second insulator layer over the first insulator layer, wherein the second insulator layer encapsulates the patterned second conductor trace layer and the second interconnect layer; and

removing a depth of the second insulator layer to expose the second interconnect layer.

22. The manufacturing method according to claim 21, further comprising:

forming an outermost patterned conductor trace layer on the last formed insulator layer;

sealing the outermost patterned conductor trace layer with an insulating layer; and

selectively exposing areas of the outermost patterned conductor trace layer for external electric connection.

23. The manufacturing method according to claim 21, wherein the size of the second insulator layer is larger than the first insulator layer and the second insulator layer encapsulates the first insulator layer in an overmolding.

24. The manufacturing method according to claim 21, wherein the size of the second insulator layer is the same as the size of the first insulator layer.

25. The manufacturing method according to claim 21, wherein after the step of grinding of the first insulator layer, the manufacturing method further comprises depositing an adhesion layer on the first insulating layer, and forming the second patterned conductor trace layer on the adhesion layer.

26. The manufacturing method according to claim 21, further comprising:

removing the sacrificial carrier to expose the first insulator layer and the patterned first conductor trace layer, wherein the patterned first conductor trace layer is leveled or recessed in the exposed surface of the first insulator layer and the edges of the patterned first conductor trace layer is defined by the first insulator layer.

27. The manufacturing method according to claim 26, wherein the sacrificial carrier is partially removed to form a plurality of openings exposing the patterned first conductor trace layer.

28. The manufacturing method according to claim 26, wherein the internal portion of the sacrificial carrier is removed to form a carrier ring around the periphery of the semiconductor substrate.

29. The manufacturing method according to claim 28, wherein the sacrificial carrier is larger than the first insulator layer and part of the carrier ring extends outside a periphery of the semiconductor substrate to define a clamping area.

30. The manufacturing method according to claim 26, further comprises sealing the exposed first insulator layer and the patterned first conductor trace layer with a soldermask layer, and exposing selected areas of the patterned first conductor trace layer through the soldermask layer for electrical connections.

31. A method of manufacturing a semiconductor package comprising:

forming a semiconductor substrate according to claim 26; wherein the patterned first conductor trace layer comprises one or more patterned conductor layouts;

mounting one or more semiconductor dies on the semiconductor substrate, wherein each semiconductor die is connected to a corresponding patterned conductor layout; and

encapsulating the semiconductor die with a molding compound.