WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a well region in a substrate, the well region including a dopant of a first conductivity type;

a semiconductor pattern on the well region, the semiconductor pattern being doped with an impurity different from the dopant of the first conductivity type;

a gate electrode on the semiconductor pattern;

a gate insulation pattern between the gate electrode and the semiconductor pattern; and

isolation patterns in the well region at opposite sides of the semiconductor pattern,

wherein a lower surface of the semiconductor pattern is in contact with the well region, and an upper surface of the semiconductor pattern is in contact with the gate insulation pattern,

wherein a doping concentration of the impurity in the semiconductor pattern increases from the upper surface of the semiconductor pattern, adjacent to the gate electrode, to the lower surface of the semiconductor pattern, adjacent to the well region, and

wherein the isolation patterns expose sidewalls, respectively, of the semiconductor pattern.

2. The semiconductor device of claim 1, further comprising:

source/drain regions at opposite sides of the gate electrode,

wherein the semiconductor pattern is between the source/drain regions; and

wherein the source/drain regions are doped with an impurity having a second conductivity type different from the first conductivity type.

3. The semiconductor device of claim 1 or claim 2:

wherein a doping concentration of the impurity in an intermediate portion of the semiconductor pattern is higher than a doping concentration in the upper surface of the semiconductor pattern and is lower than a doping concentration in the lower surface of the semiconductor pattern; and

wherein the intermediate portion of the semiconductor pattern is between the upper surface of the semiconductor pattern and the lower surface of the semiconductor pattern.

4. The semiconductor device of any one of claims 1 to 3, wherein the impurity in the semiconductor pattern includes carbon, nitrogen, and/or oxygen.

5. The semiconductor device of claim 1,

wherein the gate electrode covers the upper surface and the exposed sidewalls of the semiconductor pattern.

6. The semiconductor device of claim 5, further comprising source/drain regions on the well region at opposite sides of the gate electrode,

wherein the semiconductor pattern is interposed between the source/drain regions.

7. The semiconductor device of claim 6, wherein the source/drain regions are semiconductor epitaxial patterns formed on the well region.

8. The semiconductor device of claim 6 or claim 7, wherein the source/drain regions have a different conductivity type from the well region.

9. The semiconductor device of any one of claims 6 to 8:

wherein the sidewalls of the semiconductor pattern includes first sidewalls opposite to each other in a first direction and second sidewalls opposite to each other in a second direction crossing the first direction;

wherein the isolation patterns expose the first sidewalls, respectively, of the semiconductor pattern;

wherein the gate electrode covers the exposed first sidewalls of the semiconductor pattern; and

wherein the source/drain regions cover the second sidewalls, respectively, of the semiconductor pattern.

10. The semiconductor device of any one of claims 1 to 9:

wherein the well region includes a first well region and a second well region that have different conductivity types from each other;

wherein the semiconductor pattern includes a first semiconductor pattern on the first well region and a second semiconductor pattern on the second well region;

wherein the gate electrode includes a first gate electrode on the first semiconductor pattern and a second gate electrode on the second semiconductor pattern;

wherein the gate insulation pattern includes a first gate insulation pattern between the first gate electrode and the first semiconductor pattern and a second gate insulation pattern between the second gate electrode and the second semiconductor pattern;

wherein each of the first semiconductor pattern and the second semiconductor pattern includes the impurity;

wherein the doping concentration of the impurity in the first semiconductor pattern increases in a direction from an upper portion of the first semiconductor pattern, adjacent to the first gate electrode, to a lower portion of the first semiconductor pattern, adjacent to the first well region; and

wherein the doping concentration of the impurity in the second semiconductor pattern increases in a direction from an upper portion of the second semiconductor pattern, adjacent to the second gate electrode, to a lower portion of the second semiconductor pattern, adjacent to the second well region.

11. A semiconductor device comprising:

a well region in a substrate, the well region including a dopant of a first conductivity type;

a semiconductor pattern on the well region, the semiconductor pattern being doped with an impurity different from the dopant of the first conductivity type;

isolation patterns in the well region at opposite sides of the semiconductor pattern, the isolation patterns exposing sidewalls, respectively, of the semiconductor pattern;

a gate electrode covering the semiconductor pattern and the isolation patterns; and

source/drain regions on the well region at opposite sides of the gate electrode,

wherein the semiconductor pattern is interposed between the source/drain regions, and

wherein a doping concentration of the impurity in the semiconductor pattern increases from an upper surface of the semiconductor pattern, adjacent to the gate electrode, to a lower surface of the semiconductor pattern, adjacent to the well region.

12. The semiconductor device of claim 11, wherein the impurity includes carbon, nitrogen, and/or oxygen.

13. The semiconductor device of claim 12, wherein the semiconductor pattern includes silicon.

14. The semiconductor device of any one of claims 11 to 13:

wherein the gate electrode covers the upper surface and the exposed sidewalls of the semiconductor pattern and extends on upper surfaces of the isolation patterns.

15. The semiconductor device of any one of claims 11 to 14:

wherein the semiconductor pattern includes first sidewalls that are opposite to each other in a first direction and second sidewalls that are opposite to each other in a second direction crossing the first direction;

wherein the gate electrode extends in the first direction and covers the first sidewalls of the semiconductor pattern and upper surfaces of the isolation patterns; and

wherein the source/drain regions are spaced apart from each other with the semiconductor pattern therebetween and covers the second sidewalls of the semiconductor pattern.

16. The semiconductor device of any one of claims 11 to 15, wherein the doping concentration of the impurity in the semiconductor pattern continuously increases from the upper surface of the semiconductor pattern to the lower surface of the semiconductor pattern.

17. The semiconductor device of any one of claims 11 to 16, wherein the source/drain regions have a different conductivity type from the well region.

18. The semiconductor device of any one of claims 11 to 17, wherein uppermost surfaces of the source/drain regions are higher than the upper surface of the semiconductor pattern with respect to an upper surface of the substrate.