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(54) TELEVISION LINE-DEFLECTION CIRCUIT

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to a circuit arrangement comprising a line deflection circuit for generating a line frequency sawtooth current having a trace and a retrace period through a line deflection coil and a voltage supply circuit for providing a first voltage supply for said deflection circuit, said line deflection circuit having a resonant circuit which includes said line deflection coil, a trace capacitor and a retrace capacitor, and first switching means switchable at line frequency for applying in operation the voltage present across the trace capacitor to the line deflection coil during the trace period of the sawtooth current, said voltage supply circuit comprising a supply terminal for receiving a d.c. supply, second switching means controllable at line frequency with a duty cycle which in operation may be varied, a first and a second winding wound on a magnetic transformer core, said first winding being connected between said supply terminal and said second switching means whilst said second winding is connected through a diode to said line deflection circuit.

Such a circuit arrangement is described in an article in the publication "IEEE Transactions on Broadcast and Television Receivers", August 1972, vol. BRT-18, No: 3, at pages 177 to 182 and is the combination of a line deflection circuit and a switched voltage supply stabilising circuit, the first switching means in the deflection circuit comprising a transistor and associated diodes whilst the second switching means in the voltage supply circuit is formed by the said transistor. This known circuit arrangement has the advantage that it can be fed by an unstabilized supply voltage and can produce a stabilized deflection current and a stabilized high voltage (EHT) and possibly auxiliary voltages, which stabilization is obtained by controlling the duty cycle of the switch.

The article states that an EHT winding may be coupled with the windings which are the supply windings to produce EHT pulses of high amplitude during the retrace (flyback) time. These pulses are applied to a rectifier for generating the EHT for the acceleration anode of the television display tube. A drawback of this method of producing the EHT is that the first and second windings must be able to accumulate considerable power which requires a high inductance and therefore is expensive.

Another drawback of the circuit arrangement in the article is as follows. In practice, during the part of the trace time when the transistor does not conduct, the diode does conduct and the EHT winding is thus coupled to the second winding. During the other part of the trace time the transistor conducts and the diode does not so that the EHT winding is then coupled to the first winding. Since the leakage inductance between the EHT winding and the first winding and that between the EHT winding and the second winding are necessarily different for reasons of winding and assembly technique, the series resonant frequency of the network constituted by the leakage inductance and the capacitance to ground is different during the two parts of the trace time. As a result a higher harmonic tuning of the combined windings which can be considered to be an EHT transformer is not possible so that parasitic oscillations may be produced.

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A further drawback of this method of producing the EHT is that the voltage across the first and second windings varies with a step at the instant when the transistor is rendered conducting. The abovementioned series resonant network is thereby excited which may give rise to parasitic oscillations after the said instant. In addition, this instant, which is dependent on the supply voltage, is variable.

These drawbacks may be eliminated if the EHT winding is coupled to a separate winding which is either coupled directly or through a capacitor to the deflection network. Such an arrangement is shown in Figure 8 of the above article at page 181. During the whole of the trace time a current flows through this winding so that the leakage inductance between it and the EHT winding does not vary, whilst the voltage thereacross does not contain the step during the trace time. In producing the EHT in this way there is the drawback that the circuit arrangement not only includes the first and second windings but also an extra transformer which must be capable of handling considerable power, in colour television receiver in the order of a maximum of $25 \text{ kV} \times 2 \text{ mA} = 50 \text{ W}$ EHT power, and which is therefore an expensive component.

It is an object of the invention to provide a circuit arrangement which does not require these separate expensive components.

The invention provides a circuit arrangement comprising a line deflection circuit for generating a line frequency sawtooth current having a trace and a retrace period through a line deflection coil and a voltage supply circuit for providing a first voltage supply for said deflection circuit, said line deflection circuit having a resonant circuit which includes said line deflection coil, a trace capacitor and a retrace capacitor, and first switching means switchable at line frequency for applying in operation the voltage present across the trace capacitor to the line deflection coil during the trace period of the sawtooth current, said voltage supply circuit comprising a supply terminal for receiving a d.c. supply, second switching means controllable at line frequency with a duty cycle which in operation may be varied, a first and a second winding wound on a magnetic transformer core, said first winding being connected between said supply terminal and said second switching means whilst said second winding is connected through a diode to said line deflection circuit, a third winding wound on said magnetic core which third winding is connected to said deflection circuit and means comprising a fourth winding wound on said magnetic core for deriving a second voltage supply, said fourth winding being more closely coupled to said third winding than to said first or second windings, the arrangement being such that in operation said second switching means causes a line frequency voltage having a duty cycle which can be varied to be impressed on said first and second windings whilst said deflection circuit impresses a line frequency voltage having a retrace pulse and which does not substantially vary during the trace period on said third winding.

With the invention a voltage is present across the first and second windings which during the retrace time is proportional to the retrace pulse, during the part of the trace time when the second switching means does not conduct has a first value whilst during the rest of the trace time when the second switching means conducts has a second value. However, a voltage which is equal to the retrace pulse during the retrace time but does not substantially vary during the entire trace time is present across the third winding which is connected to the deflection network. As coupling exists between these windings due to them being wound on the same core, currents will flow through them which are dependent inter alia on the difference between the voltage across the third winding and that across the first and second windings but which do not influence these voltages so that voltages of different shapes remain present across the coupled windings. It has been found that these currents not only result in substantially no increase of the losses but that they have no detrimental influence in the case of a suitable chosen design of the arrangement because the operation of the arrangement remains unchanged in spite of the fact that one of these extra currents through the diode flows in the blocking direction and therefore might turn off this diode.

With the circuit arrangement in the above mentioned article a given minimum power has to be dissipated for its satisfactory operation. It has been found that with the circuit arrangement according to the invention this minimum power can be considerably reduced so that in theory the situation can be achieved where it derives little energy from an external d.c. supply and so producing only small losses in the arrangement. This can be obtained by suitable choice of two of the parameters determining the operation of the arrangement, namely the coupling factor and the transformation ratio between the second and third windings. The maximum intensity of the current flowing through a transistor which may be included in the first and second

switching means, i.e. at the end of the trace time, and the premagnetisation of the core can be reduced. A compromise can be found in which all requirements can be satisfied in a reasonable way.

The invention also provides a circuit arrangement comprising a line deflection circuit for generating a line frequency sawtooth current having a trace and a retrace period through a line deflection coil and a voltage supply circuit for providing a first voltage supply for said deflection circuit, said line deflection circuit having a resonant circuit which includes said line deflection coil, a trace capacitor and a retrace capacitor, and first switching means switchable at line frequency for applying in operation the voltage present across the trace capacitor to the line deflection coil during the trace period of the sawtooth current, said voltage supply circuit comprising a source of d.c. supply, second switching means controllable at line frequency with a duty cycle which in operation may be varied and a supply winding wound on a magnetic transformer core which supply winding is connected in series with said supply source and said second switching means and is additionally connected to said line deflection circuit, a further winding wound on said magnetic core which further winding is also connected to said deflection circuit, and means comprising an additional winding wound on said magnetic core for providing a second voltage supply, said additional winding being more closely coupled to said further winding than to said supply winding, the arrangement being such that in operation said second switching means causes a line frequency voltage having a duty cycle which can be varied to be impressed on said supply winding whilst said deflection circuit impresses a line frequency voltage having a retrace pulse and which does not substantially vary during the trace period on said further winding.

The above and other features of the invention will now be described in greater detail, by way of example, with reference to the accompanying drawings, in which:—

Figure 1 shows the principle circuit diagram of a first embodiment of the arrangement according to the invention,

Figure 2 shows waveforms occurring therein,

Figure 3 shows an equivalent circuit diagram of part of the arrangement according to Figure 1,

Figure 4 shows a graph which may serve in the choice of the parameters,

Figure 5 shows a variation of a current flowing in the arrangement of Figure 1,

Figure 6 shows the principle circuit diagram of a second embodiment of the arrangement according to the invention,

Figure 7 is a sketch of a transformer which may be used in the arrangement according to the invention,

Figures 8 and 9 show other embodiments of the arrangement according to the invention.

The circuit arrangement of Figure 1 includes a driver stage Dr which receives signals from a line oscillator not shown and which applies switching pulses to the base of a switching transistor Tr. One end of a primary winding L_1 of a transformer T is connected to the collector of transistor Tr which is of the npn type while the other end of winding L_1 is connected to the positive terminal of a direct voltage source B and the emitter of transistor Tr is connected to the negative terminal thereof. This negative terminal may be connected to ground of the circuit arrangement.

A trace capacitor C_t is arranged in series with the line deflection coil L_d of the circuit arrangement of Figure 1 in the television display apparatus (not shown) and a diode D_1 with the indicated conductivity direction and a retrace capacitor C_r are each arranged in parallel with the series arrangement thus constituted. Capacitor C_r may alternatively be arranged in parallel with coil L_d . The four elements only show the main components of the deflection section. This section may be provided, for example, in known manner with one or more transformers for mutual coupling of the elements, with arrangements for centering and linearity correction and the like.

A secondary winding L_2 of transformer T is arranged in series with a diode D_2 whose cathode is connected to the junction A of elements D_1 , C_r and L_d and to the anode of a diode D_3 . The cathode of diode D_2 is connected to the collector of transistor Tr. A tertiary winding L_3 of transformer T is connected through a capacitor C_1 to point A. Other windings are wound on the core of transformer T across which windings there are voltages which provide supply voltages for other parts of the television display apparatus. One of these windings, winding L_4 , is shown in Figure 1 and generates with the aid of a rectifier D_4 a positive direct voltage across a smoothing capacitance C_2 . One of these windings, for example the winding L_4 , is the EHT winding so that the voltage across capacitance C_2 is the EHT for the

acceleration anode of the display tube (not shown). The free ends of windings L_2 , L_3 and L_4 are connected to ground and the winding sense of the windings shown of transformer T is denoted by polarity dots in the Figure.

If, initially, we ignore the fact that winding L_3 is coupled to the inductive element L_1 , L_2 of the known arrangement, the described circuit arrangement operates as that of the above-mentioned publication which may be summarised as follows. For the deflection circuit transistor Tr and diodes D_1 and D_2 form the first switching means. During a first part of the line trace (scan) time, diode D_1 conducts. The voltage across capacitor C_1 is applied to deflection coil L_y through which a sawtooth deflection current i_y flows. At a given instant transistor Tr becomes conducting. When approximately in the middle of the trace time current i_y reverses its direction, diode D_1 is blocked so that current i_y then flows through the previously non-conducting diode D_2 and transistor Tr. At the end of the trace time, transistor Tr is cut off and diode D_2 again becomes non-conducting. An oscillation, the retrace (fly back) pulse, is produced across capacitor C_1 while the energy stored in transformer T and derived from source B produces a current through diode D_3 . When the voltage across capacitor C_1 has become zero again, diode D_1 becomes conducting: this is the commencement of a new trace time. Diode D_3 remains conducting until transistor Tr is rendered conducting, the energy in winding L_2 being passed on to winding L_1 . Stabilization is provided in that, for example, the voltage across capacitor C_1 is fed back to driver circuit Dr in which a comparison stage and a modulator insure that the conductivity time of transistor Tr is varied in such a manner that the said voltage and consequently the amplitude of the deflection current remain constant. Thus for the voltage supply circuit the transistor Tr forms the second switching means.

In Figure 2a the voltage v_A across capacitor C_1 , in Figure 2b the voltage v_2 at the junction of winding L_2 and diode D_3 and in Figure 2c the voltage v_0 at the collector of transistor Tr are plotted as a function of time. The symbol T_H indicates the line period while τ_1 indicates the retrace (fly back) time, τ_2 the part of the trace (scan) period $T_H - \tau_1$ when transistor Tr does not conduct and $\tau_3 = \delta T_H$ being the part of the period T_H in which the transistor does conduct. The number δ is the ratio between time τ_3 and period T_H .

During the times τ_1 and τ_2 diode D_3 conducts and voltages v_A and v_2 are equal, i.e. the retrace pulse with amplitude V during the time τ_1 and zero during the time τ_2 . At the instant when transistor Tr is rendered conducting i.e. at instant t_1 between τ_2 and τ_3 , voltage v_0 becomes substantially zero. The voltage V_B from source B is then produced across winding L_1 . If the transformer ratio between windings L_2 and L_1 i.e. the ratio between the number of turns of winding L_2 to that of winding L_1 is equal to 1:p, voltage v_2 is equal to

$$-\frac{V_B}{p}$$

during the time τ_3 . Voltage v_0 is equal to $pV_2 + V_B$ during the time τ_1 .

When V_0 is the direct voltage across capacitor C_1 , then if this capacitor has a sufficiently large capacitance, or if V_0 is the direct voltage component of the voltage across this capacitor when it has a comparatively low capacitance for the so-called S correction, V_0 is equal to the mean value of voltage v_A . In fact, a direct voltage component cannot be present across coil L_y . There applies that:

$$V_0 = \frac{1}{T_H} \int_0^{\tau_1} v_A dt$$

The mean value of the voltage across winding L_2 is also zero so that there applies that:

$$\int_0^{\tau_1} v_A dt - \frac{V_B}{p} \cdot \tau_3 = 0$$

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In the formula for V_o , the integral can be replaced so that

$$V_o T_H = \frac{V_B}{p} \cdot \tau_3, \quad \text{i.e.} \quad V_o = \frac{\delta \cdot V_B}{p} \quad (1)$$

At given values of ratios δ and p , diode D_2 would conduct during the time τ_1 . Since diode D_3 conducts during this period, windings L_1 and L_2 would be short-circuited by diodes D_2 and D_3 so that the retrace pulse across capacitor C_r would be cut off and the deflection current would be distorted. Such an effect may be obviated, for example, by providing an additional transistor cut off during the time τ_1 in series with diode D_2 . A capacitor C_3 is arranged between the ends of windings L_1 and L_2 in Figure 1 or taps thereof and this capacitor prevents parasitic oscillations which might be caused by the leakage inductance present between the windings L_1 and L_2 in such a manner that a line frequency voltage is not present across capacitor C_3 . Figure 1 shows the case where $p=1$.

Similarly as for capacitor C_1 , it may be evident that a direct voltage or a direct voltage component is present across capacitor C_1 which is equal to voltage V_o , so that the voltage across winding L_3 is substantially equal in shape to that of Figure 2a with the difference that the zero axis is shifted and has a value equal to voltage V_o . The invention is based on the recognition of the fact that windings L_1 and L_2 on the one hand and winding L_3 on the other hand may be coupled together as is the case in Figure 1, in spite of the fact that voltages having waveforms of different shapes are present across these windings, and that these shapes are not influenced by the coupling. Coupling of the windings of transformer T cannot influence the fixed voltages V_o and V_B , that is to say, voltages externally impressed. However, the currents flowing through the different windings are influenced.

Figure 3 shows an equivalent circuit diagram of a part of Figure 1. As in the mentioned publication, the coupling between windings L_1 and L_2 is very tight. Thanks to the presence of capacitor C_3 the coupling factor between these windings may be considered to be equal to 1. The coupling factor between windings L_2 and L_3 is not equal to 1 so that only a part of the tertiary winding is coupled to the secondary winding where the coupling factor is equal to 1 and is in series with an inductor Q not coupled to the secondary winding which inductor represents the leakage inductance between windings L_2 and L_3 . Thus, the equivalent circuit diagram comprises three windings l_1 , l_2 and l_3 mutually having a coupling factor of 1 and with the transformer ratio of l_1 to l_2 equal to the above-mentioned ratio p and of l_3 to l_2 equal to a number n . An inductor having a value of L_1 is shown to be in parallel across winding l_1 which value is equal to the value measured across winding L_1 in Figure 1 without a load across the other windings. The above-mentioned inductor Q in series with winding l_3 is measured across the series arrangement which value is equal to that of winding L_3 in Figure 1 without a load across the other windings. It can be derived that:

$$Q = L_3 - n^2 L_1 = L_3 (1 - k^2) \quad \text{and}$$

$$k = n \sqrt{\frac{L_1}{L_3}}$$

in which k is the coupling factor between windings L_2 and L_3 in Figure 1.

In the absence of any coupling between windings L_2 and L_3 ($k=0$) the respective currents i_{10} , i_{20} and i_{30} would flow through windings L_1 , L_2 and L_3 in which currents i_{10} and i_{20} correspond to i_1 and i_2 of the quoted publication and in which current i_{30} , likewise as current i_3 , is sawtoothed-shaped. Since windings L_2 and L_3 are coupled together, extra currents i_{1k} , i_{2k} and i_{3k} flow through the respective windings. When it is assumed that the arrangement comprises ideal inductors, capacitors and semiconductors, these extra currents do not cause any increase in losses. In practice, this increase will remain small. In addition, the above-defined parameters n and k may be chosen to be such that the operation of the arrangement is not detrimentally influenced which will be explained hereinafter.

The respective currents $i_1 = i_{10} + i_{1k}$, $i_2 = i_{20} + i_{2k}$ and $i_3 = i_{30} + i_{3k}$ actually flow through the windings l_1 , l_2 and l_3 of Figure 3. The following can be shown.

During the time τ_1 , $i_1=0$ and currents i_2 and i_3 undergo the variations

$$\Delta i_2 = - \frac{V_0 T_H}{L_1} \cdot \frac{1}{1-k^2} \left(1 - k^2 \cdot \frac{\tau_2 + \tau_3}{n T_H} \right)$$

and

$$\Delta i_3 = \frac{V_0 T_H}{L_1} \cdot \frac{k^2}{1-k^2} \left(1 - \frac{\tau_2 + \tau_3}{n T_H} \right)$$

During the time τ_2 : $i_1=0$

$$\Delta i_2 = - \frac{V_0 T_H}{L_1} \cdot \frac{k^2}{1-k^2} \cdot \frac{\tau_2}{n T_H}$$

and

$$\Delta i_3 = \frac{V_0 T_H}{L_1} \cdot \frac{k^2}{1-k^2} \cdot \frac{\tau_2}{n^2 T_H}$$

During the time τ_3 : $i_2=0$

$$\Delta i_1 = \frac{V_0 T_H}{p L_1} \cdot \frac{1}{1-k^2} \left(1 - k^2 \cdot \frac{\tau_3}{n T_H} \right) \quad (2)$$

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and

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$$\Delta i_3 = - \frac{V_0 T_H}{n L_1} \cdot \frac{k^2}{1-k^2} \left(1 - \frac{\tau_3}{n T_H} \right)$$

In order that the operation of the arrangement is not disturbed, current i_2 must always flow in the positive direction as shown by the arrow in Figure 3 in spite of the fact that the variation Δi_2 thereof is always negative in the time τ_2 . Figure 3 shows that current i_1 must therefore also be positive. Since current i_1 only flows during the time τ_3 and since the abovementioned relation (2) shows that its variation Δi_1 may be both positive and negative going during that time, the condition which must be satisfied is as follows: when $\Delta i_1 > 0$, i_1 must be larger than or equal to zero at instant t_1 which is dependent on δ and consequently on voltage V_B ; when $\Delta i_1 < 0$, i_1 must be larger than or equal to zero at the instant t_2 when the trace time ends.

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The mean value of current i_1 follows from the calculation of the power taken up by the arrangement:

$$\begin{aligned} W &= \frac{1}{T_H} \int_0^{T_H} V_B i_1 dt = \frac{V_B}{p T_H} \int_0^{\tau_3} p i_1 dt \\ &= \frac{V_B}{p T_H} \cdot i_0 \tau_3 \end{aligned}$$

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in which

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$$p i_0 = \frac{1}{\tau_3} \int_0^{\tau_3}$$

$p i_0$ = the said mean value transformed to the secondary side. Filling in formula (1) leads to:

$$p i_0 = \frac{W}{V_0}$$

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independent of parameter k .

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For the lowest possible value $\delta_{\min}$ of δ the above given condition applies:

$$p(i_0 - \frac{1}{2}\Delta i_1) \geq 0 \text{ with } \Delta i_1 > 0$$

from which

$$WL_1 = (WL_1)_0 \cdot R_1$$

while for the highest possible value $\delta_{\max}$ of δ there applies that:

$$p(i_0 + \frac{1}{2}\Delta i_1) \geq 0 \text{ with } \Delta i_1 < 0$$

from which

$$WL_1 = (WL_1)_0 \cdot R_2$$

In this formula $(WL_1)_0$ is the value of the product WL_1 for $k=0$, thus without coupling, and

$$R_1 \geq \frac{1}{1-k^2} \left(1 - k^2 \cdot \frac{\delta_{\min}}{n} \right)$$

$$R_2 \geq \frac{1}{1-k^2} \left(k^2 \cdot \frac{\delta_{\max}}{n} - 1 \right)$$

At a retrace ratio of

$$\frac{\tau_1}{T_H} = 0.2$$

$\delta_{\max}=0.8$ (transistor Tr is rendered conducting at the instant of commencement t_0 of the trace time) and $\delta_{\min}=0.4$ (instant t_1 coincides with the middle of the trace time). With these data the graph of Figure 4 can be shown in which the coefficients R_1 and R_2 are plotted as a function of n and with k as a parameter.

Figure 4 shows that for a given value of the coupling factor k values for the ratio n can be chosen which are located above the relevant curve of R_1 and to the right of the relevant curve of R_2 . The values which are given by these curves show the minimum value of the ratio of the product WL_1 for the said value of factor k and the product $(WL_1)_0$ without coupling when the arrangement can still operate in its normal manner. It is found that values of the parameters n and k can be chosen in which this ratio is less than 1. Such a case occurs, for example, with $k=0.71$ and $n \approx 0.3$ in which $R_1=R_2=0.67$ (point M) and, more in general, for $k=0.71$ for the shaded part of the graph. Larger coupling factors are possible: with $k=0.84$ and $n=0.4$, $R_1=R_2=1$ (point N) is obtained which does not result in an improvement, but does not involve a deterioration relative to the case without coupling while the deterioration is small for the case of point P for which $k=0.71$, $n=0.6$ and $R_1 \approx 1.35$. Thus it is found that parameters k and n can be chosen arbitrarily.

Physically, the fact that the minimum dissipated power W for a given L_1 (hence for a given quantity of iron and copper) may be smaller than when windings L_2 and L_3 are not coupled together and with the same L_1 can be described as follows. Without coupling, currents i_{10} and i_{30} always flow in the positive direction so that a certain dissipation is necessary, for example, by losses in deflection coil L_y and/or by a load connected to capacitor C_t . With coupling, extra currents i_{1k} and i_{3k} flow which are produced by energy accumulated in winding L_3 and which are induced in windings L_1 and L_2 , which currents may flow in the negative direction without diode D_3 being blocked. As a result, part of the energy supplied is fed back to source B again. The foregoing shows that the requirement for the dissipated power to minimum goes together with the requirement that the operation of the arrangement is not influenced by the coupling, that is to say, diode D_3 remains conducting in the time τ_2 .

Figure 5 shows the variation of current i_2 during the times τ_1 and τ_2 and of current pi_1 during the time τ_3 for different values of the ratio

$$\delta = \frac{\tau_3}{T_H}$$

i.e. for different values of supply voltage V_B . Figure 5a shows that the variation of Δi_1 in formula (2) is positive and in Figure 5c this variation is negative. Formula (2) shows that for the value of

$$\delta = \frac{n}{k^2}$$

the variation Δi_1 is zero. Current i_{p1} then retains the value i_{p0} during the time τ_3 (Figure 5b). Since this value which is the same in Figures 5a, b and c is proportional to the dissipated power W , it is very low if the power W is low. Since current i_2 becomes slightly lower after instant t_2 than i_{p0} , i_c cannot be zero but can be very small. This means that the theoretical situation is approximated in which the arrangement does not draw substantially any energy from source B while there are no losses.

Another important consideration relates to the maximum collector current of transistor Tr. At the end t_2 of the trace time, current i_y which then flows through diode D_2 and transistor Tr assumes its maximum intensity. Also the current through winding L_1 and that through winding L_3 flow through transistor Tr. During the time τ_3 , the collector current i_c is equal to

$$\begin{aligned} i_c &= i_y + i_1 + i_3 = i_y + (i_{10} + i_{1k}) + (i_{30} + i_{3k}) \\ &= i_y + (i_{10} + i_{30}) + (i_{2k} + i_{3k}) \\ &= i_{c0} + i_{ck} \end{aligned}$$

in which i_{c0} and i_{ck} represent the collector current without and with coupling between windings L_2 and L_3 . It can be shown that for a suitable choice of parameters k and n , current i_{ck} becomes zero or even negative at instant t_2 , so that the collector peak current will have a more favourable value. This resides in the fact that during the trace time the voltage across winding L_2 and consequently across winding L_3 , is square-waved, so that current i_3 is sawtooth-shaped. Parameters n and k may be chosen to be such that its intensity at instant t_2 is negative but not so much that current i_c becomes zero. In this case, ratio n must not be too small. This is in contrast with the considerations in Figure 4. This Figure shows, however, that at $n=1$ and $k=0.71$ and $k=0.5$, coefficient R_1 is equal to 1.6 and 1.2, respectively, which involves 60% and 20% more power than in the case without coupling i.e. $k=0$ and $R_1=1$. At larger values of n and $k=0.5$, coefficient R_1 cannot become larger than 1.33. A satisfactory compromise between the requirement of a low dissipation and that of a lower maximum collector current can thus be found by choosing a low k which is of course not necessary if the maximum collector current at a high k is still far below its admissible peak value.

Another advantage of the invention is that the magnetizing current of transformer T can be reduced. Without coupling, a current which assumes its maximum intensity at instant t_2 flows through winding L_1 . As a result, saturation of the magnetic material constituting the core may occur so that the inductance of winding L_1 decreases. The result is that the current flowing therethrough becomes still larger so that the collector dissipation of transistor Tr increases. However, since current i_c can be reduced at instant t_2 as a result of this coupling, this means that this saturation occurs to a lesser extent and may not even occur at all. Not only is the transistor safeguarded, but the required inductance of winding L_1 can be obtained by fewer turns and/or a core of a smaller cross-section.

EHT winding L_4 is more tightly coupled to winding L_3 than to windings L_1 and L_2 which can be realized in practice by using a core which is composed of two U-shaped cores in which windings L_1 and L_2 are provided on one leg thus formed and windings L_3 and L_4 are provided on the other leg. Consequently, a voltage is present across winding L_4 which does not undergo a sudden change at instant t_1 . Known winding methods, for example, the so-called higher harmonic tuning method may be used. In the same way, the other windings (not shown) of transformer T may be more tightly coupled to winding L_3 than to windings L_1 and L_2 .

Figure 6 shows a modification of the arrangement in which the end of EHT winding L_4 remote from diode D_4 is not connected to ground but to point A. As a result an increase in the voltage to be rectified is obtained. Taps are provided on winding L_3 between which the series network L_7 , C_1 is arranged while auxiliary voltages can be derived from other taps. One of these voltages is fed back for stabiliza-

tion purposes to the modulator present in driver circuit Dr for influencing the time τ_3 . Alternatively, an extra winding L_5 of transformer T may be used for this purpose.

In one design of transformer T in which a small coupling factor k is chosen, a transformer of small dimensions may be used employing a magnetic shunt. Figure 7 shows such a construction. The magnetic flux caused by windings L_1 and L_2 is mainly present in the left leg and in the central leg, the magnetic shunt, of the core. It may be reduced to an even larger extent in the right-hand leg on which windings L_3 and L_4 are wound, when a sufficient magnetic resistance in this right-hand leg is provided in the form of an air gap. In the same manner, an air gap may also be provided in the left-hand leg.

In one embodiment according to Figure 1, the number of turns on windings L_1 , L_2 and L_3 was 230, 230 and 140, respectively, while inductance L_1 was approximately 12 mH and the coupling factor k between windings L_2 and L_3 was approximately 0.63. The core was formed without a magnetic shunt and with two air gaps each having a width of 0.6 mm. Voltage V_0 was stabilized at 140V with a variation of voltage V_B between 230 and 345 V. The inductance of deflection coil L_y was approximately 1 mH with $C_1 \approx 680$ nF and $C_2 \approx 2 \mu F$. It is clear that the capacitance of capacitor C_1 must not be too low or otherwise the voltage across a winding coupled to winding L_3 would vary parabolically during the trace time and would therefore not be usable for trace (line scan) rectification. In this embodiment the EHT winding was tuned to the fifth harmonic.

A further optimum design of the circuit arrangement according to the invention can be obtained by using air gaps of unequal widths in Figure 7. When transformer T has equal air gaps, the inductance of windings L_2 and L_3 are proportioned as the square of their number of turns. The inductance of L_2 is dependent on the minimum dissipated power, while the number of turns on windings L_3 and L_4 is determined by the desired EHT. In case of unequal air gaps the ratio of the inductances is no longer equal to the ratio of the square of the number of turns, so that a new selectable parameter is available. This parameter can be chosen to be such that the maximum collector current of transistor Tr can be reduced whilst maintaining the advantages of the invention. To this end, the widest gap is provided on the left-hand leg on which windings L_1 and L_2 are wound. The winding L_5 across which the voltage is present which is fed back to driver circuit Dr is also provided on the same leg.

An alternative circuit arrangement to that of Figure 1 is shown in Figure 8a without the properties being changed. The collector-emitter path of a second transistor Tr' is connected in parallel with diode D_1 which together form the first switching means while the base thereof is controlled by driver circuit Dr, for example, by means of a secondary winding of a driver transformer T' another secondary winding of which controls the base of transistor Tr which transistor then forms the second switching means. Transistor Tr' provides a path for deflection current i_y during the second part of the trace time. The fact that the base of transistor Tr' receives a signal for rendering it conducting during the first half of the trace time, namely at instant t_1 , is of no importance because current i_y flows through diode D_1 until the middle of scan anyway. Transistor Tr' may be of the type in which the task of diode D_1 is fulfilled by the collector-base diode of the transistor so that diode D_1 may be omitted. Since current i_y no longer flows through diode D_2 resulting in this diode remaining blocked during the entire period, it may be omitted too.

Figure 8b shows a modification of Figure 8a in which transistor Tr' is not controlled by driver circuit Dr which might result in a too high load being placed on this circuit, but by a winding L_5 of transformer T. Winding L_5 is preferably more tightly coupled to windings L_1 , L_2 and L_3 than to windings L_3 and L_4 , for example, windings L_1 , L_2 , L_3 and L_5 being provided on one leg and windings L_3 and L_4 being provided on the other leg of transformer T, which transformer, depending on its design, may be formed with or without a magnetic shunt (in Figures 8a and 8b the core of transformer T is shown as a rectangle for the sake of clarity). Such a construction has the advantage that the deflection section of the arrangement, namely windings L_2 , L_3 , L_4 and L_5 and the components coupled thereto may be isolated from the electrical mains while the supply section thereof is not isolated. This means, for example, that the lower (dead) ends of these windings and of elements Tr', Cr, Ct, etc. are connected to ground while the dead ends of winding L_5 and of elements Tr, B, etc. are connected to the neutral line of the mains supply. In this case, capacitor C_3 (shown in broken lines) must be omitted.

In the embodiments so far described, diode D_3 is directly connected to point A. In the introduction to the publication mentioned in the preamble an embodiment is described in which the supply diode D_3 is connected to the junction of a winding

of a transformer and a load capacitor, the other end of the winding being connected to point A and that of the load capacitor being connected to ground. The operation of such an embodiment is roughly the same but has the difference that the waveforms of Figures 2b and 2c during the flyback times are replaced by square-waveforms. Since the occurring voltages are externally impressed, the invention may be used as is shown in Figure 9a. The difference between the voltages is, however, that they are larger so that the extra current produced by the coupling will be larger than in the embodiments described so far which will lead to a different choice of the parameters k and n . In Figure 9a the inductor connected between D_2 and A is inductor L_7 which is wound on the core of transformer T while C_4 is the capacitor connected to ground. Windings L_1 and L_2 on the one hand, and windings L_4 and L_7 on the other hand are tightly coupled together.

In the same way as in the embodiment of Figure 8a, a transistor Tr' may be connected in parallel with diode D_1 in Figure 9a, the diode itself being possibly replaced by the collector-base diode of the added transistor. This is shown in Figure 9b in which a winding L_4 also wound on the core of transformer T to control the base of transistor Tr' .

In Figure 9b, elements Tr , L_2 , D_2 and C_4 constitute a voltage supply source of the switched mode type. A modification thereof is shown in Figure 9c in which the voltage supply source is constituted by corresponding elements namely Tr , L_2 , D_2 and C_4 , which is not arranged in parallel but in series with the deflection section to be considered as a load. It is to be noted that when the collector voltage of transistor Tr' becomes too high as a result of a defect in transistor Tr when the collector-emitter path thereof forms a short circuit, transistor Tr' is still safeguarded because its control voltage has then been removed.

WHAT WE CLAIM IS:—

1. A circuit arrangement comprising a line deflection circuit for generating a line frequency sawtooth current having a trace and a retrace period through a line deflection coil and a voltage supply circuit for providing a first voltage supply for said deflection circuit, said line deflection circuit having a resonant circuit which includes said line deflection coil, a trace capacitor and a retrace capacitor, and first switching means switchable at line frequency for applying in operation the voltage present across the trace capacitor to the line deflection coil during the trace period of the sawtooth current, said voltage supply circuit comprising a supply terminal for receiving a d.c. supply, second switching means controllable at line frequency with a duty cycle which in operation may be varied, a first and a second winding wound on a magnetic transformer core, said first winding being connected between said supply terminal and said second switching means whilst said second winding is connected through a diode to said line deflection circuit, a third winding wound on said magnetic core which third winding is connected to said deflection circuit and means comprising a fourth winding wound on said magnetic core for deriving a second voltage supply, said fourth winding being more closely coupled to said third winding than to said first or second windings, the arrangement being such that in operation said second switching means causes a line frequency voltage having a duty cycle which can be varied to be impressed on said first and second windings whilst said deflection circuit impresses a line frequency voltage having a retrace pulse and which does not substantially vary during the trace period on said third winding.

2. A circuit arrangement as claimed in Claim 1, in which one end of said third winding is connected to said deflection circuit whilst its other end is connected through a capacitor to a point of reference potential, the terminal of said diode remote from said second winding being connected to the junction of said third winding and said capacitor.

3. A circuit arrangement as claimed in Claim 1 or 2, in which said first switching means comprises a second diode in parallel with the series arrangement of a third diode and the collector-emitter path of a transistor, the parallel connection being such that in operation the voltage present across said trace capacitor is applied to said line deflection coil during one part of said trace period through said second diode and during the remaining part of said trace period through said series arrangement, the said second switching means comprising the said transistor.

4. A circuit arrangement as claimed in Claims 1, 2 or 3, in which one end of said fourth winding is connected to a rectifier means whilst its other end is connected to said deflection circuit.

5. A circuit arrangement as claimed in Claim 1 or 2, in which said first switching means comprises diode means in parallel with a first transistor, the parallel con-

of a transformer and a load capacitor, the other end of the winding being connected to point A and that of the load capacitor being connected to ground. The operation of such an embodiment is roughly the same but has the difference that the waveforms of Figures 2b and 2c during the flyback times are replaced by square-waveforms. Since the occurring voltages are externally impressed, the invention may be used as is shown in Figure 9a. The difference between the voltages is, however, that they are larger so that the extra current produced by the coupling will be larger than in the embodiments described so far which will lead to a different choice of the parameters k and n. In Figure 9a the inductor connected between D₂ and A is inductor L₇ which is wound on the core of transformer T while C₄ is the capacitor connected to ground. Windings L₁ and L₂ on the one hand, and windings L₄ and L₇ on the other hand are tightly coupled together.

In the same way as in the embodiment of Figure 8a, a transistor Tr' may be connected in parallel with diode D₁ in Figure 9a, the diode itself being possibly replaced by the collector-base diode of the added transistor. This is shown in Figure 9b in which a winding L₆ also wound on the core of transformer T to control the base of transistor Tr'.

In Figure 9b, elements Tr, L₂, D₂ and C₄ constitute a voltage supply source of the switched mode type. A modification thereof is shown in Figure 9c in which the voltage supply source is constituted by corresponding elements namely Tr, L₂, D₂ and C₄ which is not arranged in parallel but in series with the deflection section to be considered as a load. It is to be noted that when the collector voltage of transistor Tr' becomes too high as a result of a defect in transistor Tr when the collector-emitter path thereof forms a short circuit, transistor Tr' is still safeguarded because its control voltage has then been removed.

WHAT WE CLAIM IS:—

1. A circuit arrangement comprising a line deflection circuit for generating a line frequency sawtooth current having a trace and a retrace period through a line deflection coil and a voltage supply circuit for providing a first voltage supply for said deflection circuit, said line deflection circuit having a resonant circuit which includes said line deflection coil, a trace capacitor and a retrace capacitor, and first switching means switchable at line frequency for applying in operation the voltage present across the trace capacitor to the line deflection coil during the trace period of the sawtooth current, said voltage supply circuit comprising a supply terminal for receiving a d.c. supply, second switching means controllable at line frequency with a duty cycle which in operation may be varied, a first and a second winding wound on a magnetic transformer core, said first winding being connected between said supply terminal and said second switching means whilst said second winding is connected through a diode to said line deflection circuit, a third winding wound on said magnetic core which third winding is connected to said deflection circuit and means comprising a fourth winding wound on said magnetic core for deriving a second voltage supply, said fourth winding being more closely coupled to said third winding than to said first or second windings, the arrangement being such that in operation said second switching means causes a line frequency voltage having a duty cycle which can be varied to be impressed on said first and second windings whilst said deflection circuit impresses a line frequency voltage having a retrace pulse and which does not substantially vary during the trace period on said third winding.

2. A circuit arrangement as claimed in Claim 1, in which one end of said third winding is connected to said deflection circuit whilst its other end is connected through a capacitor to a point of reference potential, the terminal of said diode remote from said second winding being connected to the junction of said third winding and said capacitor.

3. A circuit arrangement as claimed in Claim 1 or 2, in which said first switching means comprises a second diode in parallel with the series arrangement of a third diode and the collector-emitter path of a transistor, the parallel connection being such that in operation the voltage present across said trace capacitor is applied to said line deflection coil during one part of said trace period through said second diode and during the remaining part of said trace period through said series arrangement, the said second switching means comprising the said transistor.

4. A circuit arrangement as claimed in Claims 1, 2 or 3, in which one end of said fourth winding is connected to a rectifier means whilst its other end is connected to said deflection circuit.

5. A circuit arrangement as claimed in Claim 1 or 2, in which said first switching means comprises diode means in parallel with a first transistor, the parallel con-



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nection being such that in operation the voltage present across said trace capacitor is applied to said line deflection coil during one part of said trace period through said diode means and during the remaining part of said trace period through the collector-emitter path of said first transistor, the second switching means comprises a second transistor.

6. A circuit arrangement as claimed in Claim 5, in which said diode means comprises the base-collector junction of said first transistor.

7. A circuit arrangement as claimed in Claim 5 or 6, in which the base electrodes of said first and second transistors are adapted to be controlled from separate windings on a driver transformer.

8. A circuit arrangement as claimed in Claim 5 or 6, in which the base electrode of said first transistor is adapted to be controlled from a fifth winding wound on said magnetic core.

9. A circuit arrangement as claimed in any of the preceding claims, in which the duty cycle of said second switching means is controlled from a modulator, which modulator is connected to a further winding wound on said magnetic core.

10. A circuit arrangement as claimed in any of the preceding claims, in which means are provided to reduce the magnetic coupling between said first and third windings.

11. A circuit arrangement as claimed in any of the preceding claims, in which said magnetic core has a plurality of legs, said first and third windings being wound on first and second legs respectively.

12. A circuit arrangement as claimed in Claim 11 in which the first leg of said core carries said first and second windings whilst the second leg of said core carries said third and fourth windings.

13. A circuit arrangement as claimed in Claim 12, in which either said first or said second leg is provided with an air gap.

14. A circuit arrangement as claimed in Claim 12, in which said first and second legs are each provided with an air gap, the air gap in said first leg being wider than that in said second leg.

15. A circuit arrangement as claimed in Claim 11, 12, 13 or 14, in which said magnetic core has three parallel legs, the outer pair of which constitute said first and second legs whilst the central leg constitutes a magnetic shunt.

16. A circuit arrangement comprising a line deflection circuit for generating a line frequency sawtooth current having a trace and a retrace period through a line deflection coil and a voltage supply circuit for providing a first voltage supply for said deflection circuit, said line deflection circuit having a resonant circuit which includes said line deflection coil, a trace capacitor and a retrace capacitor, and first switching means switchable at line frequency for applying in operation the voltage present across the trace capacitor to the line deflection coil during the trace period of the sawtooth current, said voltage supply circuit comprising a source of d.c. supply, second switching means controllable at line frequency with a duty cycle which in operation may be varied and a supply winding wound on a magnetic transformer core which supply winding is connected in series with said supply source and said second switching means and is additionally connected to said line deflection circuit, a further winding wound on said magnetic core which further winding is also connected to said deflection circuit, and means comprising an additional winding wound on said magnetic core for providing a second voltage supply, said additional winding being more closely coupled to said further winding than to said supply winding, the arrangement being such that in operation said second switching means causes a line frequency voltage having a duty cycle which can be varied to be impressed on said supply winding whilst said deflection circuit impresses a line frequency voltage having a retrace pulse and which does not substantially vary during the trace period on said further winding.

17. A circuit arrangement as claimed in Claim 16, in which said first switching means comprises diode means in parallel with a first transistor, the parallel connection being such that in operation the voltage present across said trace capacitor is applied to said line deflection coil during one part of said trace period through said diode means and during the remaining part of said trace period through the collector-emitter path of said first transistor, the second switching means comprises a second transistor, one end of said further winding being connected to said deflection circuit whilst its other end is connected through a capacitor to a point of reference potential, one end of said supply winding being connected to the junction of said further winding and said capacitor, whilst its other end is connected to said second transistor and through a further diode to said point of reference potential.



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18. A circuit arrangement comprising a line deflection circuit and a voltage supply circuit, substantially as herein described with reference to the accompanying drawings.

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19. Television display apparatus provided with a circuit arrangement as claimed in any of the preceding claims.

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