SUB-HALF-MICRON MULTI-LEVEL INTERCONNECTION STRUCTURE AND PROCESS THEREOF

ABSTRACT

The present invention relates to the field of semiconductor manufacturing, and more specifically to methods of forming sub-half-micron multi-level interconnect structures for integrated circuits. The inventive structure and process are spike free and that has resulted in improved circuit performance, reliability and process yields. The inventive structure and process have a plurality of insulator layers where each of the adjoining insulator layers are of a different material.

Fig. 3