Radio Frequency Power Delivery System

BACKGROUND

[0001] Various approaches exist for providing RF power to dynamic loads. RF generators provide power to dynamic loads typically at frequencies between about 400 kHz and about 200 MHz. Frequencies used in some scientific, industrial and medical applications are approximately 2 MHz, 13.56 MHz and 27 MHz.

[0002] As shown in FIG. 1A, one system 100 for providing RF power to dynamic loads (i.e., a plasma load 140) involves a fixed frequency RF generator 110 and a two-axis tunable matching network 120 connected by a 50 Ω transmission line 130. The tunable matching network 120 includes a series motorized vacuum variable capacitor 122 and inductor 124 and a shunt motorized vacuum variable capacitor 126. The algorithm used to determine the series and shunt capacitance is based on impedance measurements typically made using a magnitude and phase detector 150. Independent power control is based on power measurements at the RF generator 110. The power control loop 160 and impedance control loop 162 are independent.

[0003] As shown in FIG. 1B, another system 100' for providing RF power to dynamic loads involves a fixed element matching network 120' fed by an RF generator 110 and connected by a 50 Ω transmission line 130. The fixed element matching network 120' includes a series capacitor 122 and inductor 124 and a shunt capacitor 126. The frequency of the RF generator 110 can be tuned to a certain range (e.g., 13.56 MHz ±5%). The RF generator 110 frequency command is based on the value of voltage standing wave ratio (VSWR). The independent power loop and VSWR (impedance) control loop 160' are based on measurements at the output of the RF generator 110.

[0004] As shown in FIG. 1C, another system 100'' for providing RF power to dynamic loads involves an integrated RF generator-impedance matching network 120''. The RF generator-impedance matching network 120'' includes a series capacitor 122 and inductor 124 and a plurality of shunt capacitor 126a...126n. The shunt capacitor 126a...126n are coupled to a switching circuit 127a...127n that couples and decouples the capacitors 126 to ground. The power control and frequency control 160'' of the system 100'' are not conducted simultaneously.

[0005] As shown in FIG. 1D, another system 100''' for providing RF power to dynamic loads utilizes a one-input multi-output power splitter 132. The system includes an RF

power delivery system 130, a power splitter 132, and a plurality of dynamic loads 140a, 140b...140n, generally 140. The RF power delivery system 130 outputs a power *p* to the power splitter 132. The power splitter 132 provides power having the same frequency and phase to one or more of the dynamic loads 140. The power delivered to each load (140a ... 140n) is a fraction of the total RF generator output power *p* (e.g., power equal to p/a_1 to Load #1 140), reducing the maximum available power supplied to any individual load.

SUMMARY

[0006] These prior art techniques and methods have disadvantages. Higher cost is typically associated with prior art techniques and methods due to the need for at least two separate modules: 1) the RF generator/amplifier and 2) the impedance matching network, which are to be connected via a transmission line. Furthermore, each module requires a RF voltage/current sensor or a magnitude/phase detector.

[0007] The advent of sub-45nm manufacturing has placed plasma processing tools under pressure to meet aggressive plasma process objectives. First, extremely short process steps that are needed for Atomic Layer Deposition (ALD). The short process steps require fast stabilization of the reactants and plasma. Second, rapidly alternating deposition and etch steps are needed to meet CD objectives. The rapidly alternating deposition and etch steps often incorporate highly electronegative gases that dramatically change plasma impedance. Third, to optimize process conditions in multi-step recipe chains, operation within a wide range of power settings is required. The wide range of power settings can require that a single generator operate over a wide power band, for example 5 to 2000 W. Fourth, control of wafer bias voltage, in order to control ion bombardment energy, requires external feedback and control of a bias RF power supply. Fifth, the use of a pulsed power output can yield a number of potential advantages including improved etch selectivity, improved etch rate and uniformity, improved deposition rate and uniformity, reduced particle generation and control of wafer charging to prevent arcing or reduce sidewall damage. Given the above mentioned requirements, it is essential that the next generation RF power source be able to ensure process stability and repeatability.

[0008] Plasma impedance is a function of the power delivered to the plasma. Furthermore, the power delivered by the RF generator is a function of the impedance

"seen" by the generator. As a result, a clear circular interdependence exists between delivered power and load impedance yielding a multi-input-multi-output (MIMO) system with cross-coupling. In prior art systems, the RF generator control loop and the impedance matching control loop are independent and thus cannot compensate for the cross-coupling between power control and impedance matching control loops. This leads to poor closed-loop performance.

[0009] Additionally, prior art RF amplifier's are typically regulated using either a purely analog control system or a purely digital control system. The purely analog control system has substantial performance degradation in the presence of nonlinearities and drifting components in the system, while the purely digital control system typically has insufficient phase margin. Thus, it is difficult to simultaneously achieve sufficient phase margin, high gain, and high bandwidth.

[0010] The dynamic response of any controlled system is only as fast as the slowest functional module (sensor, actuator, or control system parameters). In prior art systems, the slowest functional module is typically the DC power supply. Specifically, the DC power supplied to the input of the RF power amplifier usually includes a large electrolytic capacitor that is used to filter higher frequencies. The downside of using such a filter network is that the dynamic response (e.g., response to a step change in power command) is slow regardless of the control update rate. The system is therefore unable to sufficiently compensate for plasma instabilities.

[0011] In systems that use a vacuum capacitor driven by motors, the response time is on the order of hundreds of milliseconds. Owing to the fact that plasma transients (sudden and rapid change of impedance) of interest occur within hundreds of microseconds, the vacuum capacitor cannot be used to match load changes attributed to plasma transients.

[0012] Control algorithms for matching networks used in the prior art have relied upon the real and imaginary components of the measured impedance. Impedance measurement-based matching control suffers from an inherent disadvantage. For example, a change in shunt capacitance to correct or modify the real component of the impedance results in an undesirable change in the imaginary component of the impedance. Similarly, a change in the series capacitance or frequency to correct or modify the imaginary component of the impedance results in an undesirable change in the real component of the impedance. The matrix that relates the controlled variable vector (formulated by the real and imaginary components of the impedance) and the controlling

variable vector (formulated by the shunt and series capacitance or the shunt capacitance and frequency) is non-diagonal. Impedance measurement-based control algorithms are therefore not effective. Control algorithms based on the impedance formulated by using magnitude and phase measurements of the impedance are similarly ineffective.

[0013] Calibration methods for prior art systems calibrate the RF impedance analyzer or VI probe at the input of the electronic matching network. These calibration methods assume the power loss in the electronic matching network is fixed for all states of the electronic matching network and operating frequencies. However, the losses of the electronic matching network contribute significantly to the overall system operation.

[0014] Additionally, methods for driving multiple loads for prior art systems place constraints on the thermal and voltage/current handling capacities of matching networks at a higher power because the power delivered to a specific load is limited by a power rating of an RF generator and the ratio of a power splitter. Thus, independent control of power delivered to each load is not possible because the power splitter ratios are fixed.

[0015] Accordingly, a need therefore exists for improved methods and systems for controlling power supplied to a dynamic plasma load and the losses associated therewith.

[0016] There is provided a system for delivering power to a dynamic load. The system includes a power supply providing DC power having a substantially constant power open loop response, a power amplifier for converting the DC power to RF power, a sensor for measuring voltage, current and phase angle between voltage and current vectors associated with the RF power, an electrically controllable impedance matching system to modify the impedance of the power amplifier to at lease substantially match an impedance of a dynamic load, and a controller for controlling the electrically controllable impedance matching system. The system further includes a sensor calibration measuring module for determining power delivered by the power amplifier, an electronic matching system calibration module for determining power delivered to a dynamic load, and a power dissipation module for calculating power dissipated in the electrically controllable impedance matching system.

[0017] In one embodiment, the electrically controllable impedance matching system can include an inductor, a capacitor in series with the inductor, and a plurality of switched capacitors in parallel with the dynamic load. The inductor can be a multiple tap-type inductor or a variable-type inductor. Each of the plurality of switched capacitors can be in series with a switch and an additional capacitor. In another embodiment, the

electrically controllable impedance matching system can include a capacitor, and a plurality of switched capacitors in parallel with the dynamic load, wherein each of the plurality of capacitors is in series with a switch and an additional capacitor. In yet another embodiment, the electrically controllable impedance matching system can control the frequency of the impedance matching between the power amplifier and the dynamic load.

[0018] In one embodiment, the controller can control the electrically controllable impedance matching system for simultaneous control of conductance and susceptance associated with the impedance between the power amplifier and the dynamic load. In another embodiment, the controller can simultaneously control RF power frequency, RF power magnitude and the impedance between the power amplifier and the dynamic load. In yet another embodiment, the controller can control the electrically controllable impedance matching system for regulating conductance and susceptance to setpoints that stabilize an unstable dynamic load.

[0019] The power dissipated in the electrically controllable impedance matching system is the difference between the power delivered by the power amplifier and the power delivered to the dynamic load. The power delivered to the dynamic load is a sum of the power delivered to a resistive load and the power dissipated inside the load simulator.

[0020] The sensor calibration measuring module calibrates the sensor into a resistive load, wherein the resistive load is 50 Ω. The electronic matching module calibrates an output of the electrically controllable impedance matching system into a load simulator. The load simulator can be an inverse electrically controllable impedance matching system. The electronic matching system calibration module can include a power meter calibration module for determining power delivered to a resistive load; and a load simulator calibration module for determining power dissipated inside the load simulator. The resistive load can be 50 Ω. The radio frequency power delivery system provides at least the following advantages over prior art systems. The system can enhance power setpoint regulation, impedance matching, and load disturbance mitigation using high-speed (e.g., in excess of 50 kHz in one embodiment) digital multi-input-multi-output (MIMO) control. The system can operate in the presence of transient changes in plasma load properties and under conditions involving fast plasma stabilization. The system can provide a RF power delivery system that is robust to transients during startup of the system. The system can provide a high power step-up ratio, wherein the high power step-

up ratio is 100 (e.g., 15W to 1500 W). The system can measure power delivered to the load connected to the output of the integrated generator system. The system can allow for regulation of power that is independent of the power loss variation associated with the state/value of various controlled variables. The system can eliminate the need for recipe-based calibration for plasma loads.

[0021] There is provided a hybrid system for delivering power to a load. The system includes a power converter system, an outer loop coupled to the power converter system that provides a gain-bandwidth and a phase margin for substantially maintaining stability of output power, and a inner loop coupled to the power converter system for compensating nonlinearities in the power converter system.

[0022] In one embodiment, the outer loop can be an analog control loop. The inner loop can be a digital control loop. In another embodiment, the analog control loop includes an analog control, and an output conditioning block for regulating output power.

[0023] In one embodiment, the digital control loop includes an analog-to-digital converter for converting an analog measurement taken at the power converter to a digital measurement for determining a digital current set point, a digital control to output the digital current set point for determining a power width modulation signal, and a digital-to-analog converter for converting the digital current set point to an analog current set point for determining the power width modulation signal for regulating output power. In another embodiment, the analog control loop outputs the power width modulated signal based on the analog current set point and an analog measurement taken at the power converter system for regulating output power.

[0024] In one embodiment, the power converter system includes a DC source, and a RF power amplifier. A RF power measurement taken at the RF power amplifier can be digitized by the analog-to-digital converter to produce a digital RF power measurement for determining a pulse width modulation signal for regulating output power. The digital control outputs a digital current set point for determining the pulse width modulation signal for regulating output power. The digital current set point can be converted to a analog current set point for determining the pulse width modulation signal for regulating output power. The analog control loop outputs the power width modulated signal based on the analog current set point and an analog current set point measurement taken at the DC source for regulating output power.

[0025] There is provided a digital and analog hybrid method for delivering power to a load. The method involves providing a gain-bandwidth and a phase margin for substantially maintaining stability of an output power, and compensating for nonlinearities in the in the output power.

[0026] In one embodiment, the method involves measuring delivered RF power signal, converting the measured delivered RF power from an analog signal to a digital delivered RF power signal, and determining a digital current set point from the digital delivered RF power signal and a RF power set point. In another embodiment, the method involves converting the digital current set point from a digital signal to an analog current set point signal, measuring DC current at a power supply, and determining a duty cycle command from the analog current set point signal and the DC current. In another embodiment, the method involves determining a pulse width modulation signal from the duty cycle command, and

regulating the power supply with the pulse width modulation signal.

[0027] There is provided a system for delivering synchronous power. The system includes a master power system having a maximum power that delivers power to a first dynamic load; and a slave power system having a maximum power equal to the maximum power of the master power system and delivers power having a phase equal to a phase supplied by the master power system to a second dynamic load.

[0028] In one embodiment, the master power system includes a DC source for supplying power, a RF power amplifier with phase compensation for supplying power with a substantially constant phase, a VI probe for monitoring the phase of the RF power amplifier output, and an electronic matching system for matching the phase of the RF power amplifier and the load. In another embodiment, the output the master power system delivers to the load depends on the output of the VI probe. In yet another embodiment, the RF power amplifier with phase compensation includes a phase compensator circuit for supplying a phase command to a RF power amplifier to compensate for an arbitrary phase shift, and

a phase detector for detecting the phase of the output power.

[0029] In one embodiment, the slave power system includes a DC source for supplying power, a RF power amplifier with phase compensation for supplying power with a substantially constant phase, a VI probe for monitoring the phase of the RF power amplifier output, and an electronic matching system for matching the phase of the RF

power amplifier and the load. In another embodiment, the RF power amplifier with phase compensation includes a phase compensator circuit for supplying a phase command to a RF power amplifier to compensate for an arbitrary phase shift, and a phase detector for detecting the phase of the output power. In another embodiment, the master power system can be 180 degrees out of phase with the slave power system. In yet another embodiment, the master power system controls two or more slave power systems to deliver power with an amplitude and phase equal to the amplitude and phase of the master power system to two or more loads.

[0030] There is provided a method for delivering synchronous power. The method involves delivering power and phase to a first load, and delivering power and phase substantially equal to the power and phase delivered to the first load to a second load.

[0031] In one embodiment, the method involves compensating for an arbitrary phase shift in the phase of the output to the first load, and substantially maintaining the phase of the output to the first load. In another embodiment, the method involves compensating for an arbitrary phase shift in the phase of the output to the second load, and substantially maintaining the phase of the output to the second load. In another embodiment, the method involves delivering power with an amplitude and phase equal to the amplitude and phase of the first load to one or more loads.

[0032] There is provided a digital and analog hybrid system for delivering power to a load. The system includes means for providing a gain-bandwidth and a phase margin for substantially maintaining stability of output power, and means for compensating for nonlinearities at the load.

[0033] There is provided a system for delivering synchronous power. The system includes means for delivering power to a first dynamic load, and means delivering power having a phase equal to phase of the first dynamic load to a second dynamic load.

[0034] There is provided a method for delivering power to a dynamic plasma load. The method involves determining a switch of reactant gases that generate a plasma, calculating a change in output power required to sustain a plasma load with the switched reactant gases,

supplying power equal to a power required to sustain the plasma load with the switched reactant gases, and supplying power to the plasma load faster than the reactant gases change in the plasma .

BRIEF DESCRIPTIONS OF THE DRAWINGS

[0035] The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

[0036] FIG. 1A is a diagram of an RF power delivery system having a two-axis tunable matching network according to the prior art;

[0037] FIG. 1B is a diagram of an RF power delivery system having a fixed matching network according to the prior art;

[0038] FIG. 1C is a diagram of an RF power delivery system having an integrated RF generator-impedance matching network according to the prior art;

[0039] FIG. 1D is a diagram of an RF power delivery system having a one input multiple output splitter according to the prior art;

[0040] FIG. 2 is a module-based diagram of the On-Chamber RF power delivery system;

[0041] FIG. 3 is a plasma stability graph;

[0042] FIG. 4 is one embodiment of a fast DC bus of FIG. 2;

[0043] FIG. 5 is one embodiment of an RF impedance analyzer or VI Probe of FIG. 2

[0044] FIG. 6 is one embodiment of an electronic matching network of FIG. 2;

[0045] FIG. 7 is one embodiment of a module-based diagram of a DSP compensator board of FIG. 2;

[0046] FIG. 8 is a block diagram for calibrating the On-Chamber RF power delivery system;

[0047] FIG. 9A is one embodiment for calibrating a power meter to a 50 Ω calorimeter power reference;

[0048] FIG. 9B is one embodiment for calibrating a load simulator to a DC power reference;

[0049] FIG. 9C is one embodiment for calibrating an RF impedance analyzer into a 50 Ω load;

[0050] FIG. 9D is one embodiment for calibrating power delivered into the load simulator;

[0051] FIG. 11 is one embodiment of a master-slave RF power delivery system;

[0052] FIG. 12 is one embodiment of a master-slave RF power delivery system having phase compensation;

[0053] FIG. 12A is one embodiment of a master-slave RF power amplifier having phase compensation;

[0054] FIG. 13A is one embodiment of a master-slave RF power delivery system having phase compensation in an in-phase configuration;

[0055] FIG. 13B is one embodiment of a master-slave RF power delivery system having phase compensation in an out-of-phase configuration;

[0056] FIG. 14 is one embodiment of an analog-digital hybrid control loop for a power converter;

[0057] FIG. 15 is one embodiment of an On Chamber RF power delivery system analog-digital hybrid control loop; and

[0058] FIG. 16 is an circuit diagram of a compensation network.

DETAILED DESCRIPTION

[0059] Generally, an integrated radio frequency (RF) power delivery system is provided for dynamic load applications (e.g., inductive and/or capacitive plasma load). Figure 2 is an illustration of the integrated radio frequency (RF) power delivery system 200. Representative functional modules of the integrated system 200 include a fast DC bus 210, an RF power amplifier ("PA") 220, a digital signal processor ("DSP") compensator board 230, an RF impedance analyzer or VI probe 240, and an electronic matching network 250. The system 200 is coupled to a plasma load 260. It should be understood by one skilled in the art that the integrated system 200 can be implemented for a wide range of resistive and reactive loads.

[0060] Generally, the fast DC bus 210 delivers DC power to the power amplifier 220. The power amplifier 220 converts the DC power from the fast DC bus 210 to an RF power at a frequency. The electronic matching system 250 switches shunt capacitors (not shown) to match the impedance between the power amplifier 220 and the plasma load 260 to facilitate stable and maximum power transfer from the power amplifier 220 to the plasma load 260. The DSP compensator board 230 controls the operation of the system 200 based on measurements received from the fast bus controller 212 and RF impedance analyzer 240. The RF impedance analyzer 240 measures the RMS voltage, RMS current,

and phase angle between the RF voltage and current vectors. Based on these measurements, relevant RF parameters are computed by the DSP compensator board 230. These parameters include, but are not limited to impedance vector $\bar{z}$, admittance vector $\bar{y}$, delivered power P_{del}, and voltage-standing wave ratio ("VSWR"). Typical operations of the DSP compensator board include power setpoints through the fast bus controller 212, RF power frequency setpoints through the power amplifier driver 222, and switching frequency through the electronic match controller 252.

[0061] In one aspect, the system 200 achieves simultaneous power and impedance regulation. Independent susceptance regulation allows for the implementation of a frequency control algorithm based only on the deviation of the conductance from the conductance setpoint. As a result, both control loops can be operated simultaneously and at high-speed resulting in improved robustness. Further, well-known instabilities for electronegative plasmas at low-pressure (e.g., SF6 at 5mT at 300W as illustrated in Figure 3) can be stabilized by setting arbitrary conductance and susceptance setpoints in conjunction with operation of the Fast DC bus 210.

[0062] Additionally, the use of a plasma recipe can result in a varying plasma load 260. The plasma recipe requires plasma gas transitions according to the recipe steps. During gas transitions a physical change over of reactant species that create plasma happens on a timescale of tens of milliseconds. The system 200 can adjust the power output to the plasma load 260 at least five times faster that the plasma load 260 is changing. In some embodiments, the system 200 can adjust the power output to the plasma load 260 ten times faster than the plasma load 260 is changing. The power output adjustment can occur within one to two milliseconds.

[0063] FIG. 4 is a diagram of a partial resonant inverter power supply type fast DC bus 210. The fast DC bus 210 provides process stability due to its associated constant power open loop response. The fast DC bus 210 improves FET utilization over the entire load space which results in more power being delivered to the load with the same PA 220 (FIG. 2). The fast DC bus 210 has a fast response rate allowing it to deliver increased power to the plasma so it does not extinguish while also allowing the flexibility to reduce the bus voltage to ensure the FETs on the PA 220 operate in a safe mode. Other types of topologies can for the fast DC bus 210 can be used. See for example, co-pending continuation-in-part application it's parent U.S. Application Serial No. 10/947,397 filed

September 22, 2004, the entire teaching of each application are herein incorporated by reference.

[0064] In one embodiment, the fast DC bus can be a partial resonant inverter 210 that includes a pair of switches (MOSFETs) 302a, 302b, an inductor (L) 306, a capacitor (C) 308, and four diodes 310a, 310b, 310c, and 310d. In operation, the partial resonant inverter 300 converts the input voltage into a square wave or other known type DC wave form. The square wave is passed through the inductor 306 and capacitor 308, the combination of which form an LC filter, clamped by the diodes 310c, 310d, coupled and rectified by a transformer rectifier 304 and filtered to obtain a desired DC voltage (power setpoint). The DC power setpoint is provided from the DSP compensator board 230 (FIG. 2). The desired impedance setpoint can be specified in terms of its vector inverse (referred to as admittance) and which constitutes simultaneous regulation of conductance to an arbitrary conductance setpoint and regulation of susceptance to an arbitrary susceptance setpoint. The output of the partial resonant inverter 300 (DC-DC converter) is connected to DC input of the RF power generator/amplifier 220.

[0065] In operation, the capacitor 308 is periodically charged to an input rail voltage (+Vin) and discharged while the capacitor current is passed via the plasma load 260 (FIG. 2). Every charge or discharge cycle, the energy deposited in the resistive load is equal to $CV_{in}^2/2$, independent of load resistance. Thus, the power is equal to $F_{SW} \times CV_{in}^2/2$, where F_{SW} is the switching frequency and V_{in} is the input voltage. The inductor 306 ensures that the capacitor 308 is fully charged and discharged in finite time. One advantage of the partial resonant inverter 210 design is the ability to control the output voltage by varying either V or/and F_{sw}.

[0066] FIG. 5 is a diagram of one embodiment of an RF impedance analyzer or VI Probe 240. The VI Probe 240 includes a DC power supply 242, an analysis board assembly 244, and a probe head assembly 246. The analysis board assembly 244 receives low-level RF signals from the probe head assembly 246. The probe head assembly 246 provides two voltage outputs: 1) a voltage representation of the time varying electric field present in the probe head assembly 246 (voltage signal); and 2) a voltage representation of the time varying magnetic field present in the probe head assembly 246 (current signal). The analysis board assembly 244 receives and processes the two voltage outputs of the probe head assembly 246 and outputs the RF parameters to the DSP compensator board 230

(FIG. 2). MKS Instruments, Inc. VI-Probe-4100 and VI-Probe-350 are exemplary analyzers that can be used for this purpose.

[0067] FIG. 6 is a diagram of one embodiment of an electronic matching network 250. In one embodiment, the electronic matching 250 includes an inductance 254 in series with the load 260 (e.g., a compact inductor with multiple tap points), a fixed or variable series-padding capacitor 252, and field effect transistors ("FET's") 256a...256n that switch one or more upper capacitors $C_{tu}(i)$ 258a...258n to a corresponding lower capacitor $C_{td}(i)$ 258a'...258n', which is terminated to ground. In some embodiments, the electronic matching 250 network does not include the inductance 254 in series with the load 260. Other types of electronic matching networks can be used. See for example, U.S. Patent No. 6,887,339, the entire teaching of which is herein incorporated by reference.

[0068] FIG. 7 shows a module-based diagram of a DSP compensator board 230. The DSP compensator board 230 incorporates both a digital signal processor ("DSP") and a field programmable gate array ("FPGA"), and together controls the entire integrated system 200. The DSP compensator board includes an admittance compensation module 232, a frequency control module 234, an electronic match control module 236, an RF power computation module 237, and an RF power control module 238. Generally, the DSP compensator board receives the output from the VP probe 240. The admittance computation module 232 uses the VI probe outputs to calculate the admittance of the system 200. The frequency control module 234 uses the admittance to vary the frequency of the power amplifier 220. The electronic match control module 236 uses the admittance to switch the FETs 256 of the electronic matching network 250 on or off. The RF power computation module 237 uses the VI probe outputs to calculate the RF power of the system 200. The RF power control module 234 uses the RF power computation to regulate the power supplied from the fast DC bus power 210. A more detailed description of the operation of the system 200 is set forth below.

[0069] One embodiment of the power regulation objective and algorithm is set forth below: The objective is to regulate the delivered power P_{del} to a user-defined setpoint P_{sp}. To ensure smooth transitions, trajectory generators are used. In one embodiment, a first-order trajectory is generated as follows:

$$\frac{dP_t}{dt} = \frac{1}{\tau_t}\left(P_t(t) - P_{sp}\right) \qquad \text{EQN. 1}$$

where τ_t is the trajectory time constant and P_t is the desired power trajectory. The delivered-power control algorithm, in terms of the change in power commanded to the Fast Bus, is given by the following relationship:

$$P_{cmd} = k_p(P_t - P_{del}) + k_i \int (P_t - P_{del})dt \qquad \text{EQN. 2}$$

where k_p and k_i are the proportional and integral gains, respectively.

[0070] Admittance regulation objective: A normalized admittance vector is defined as follows: $\bar{y} = g + jb$ where g is the normalized conductance and b is the normalized susceptance. The impedance matching control objective is formulated as follows: $g \to g_{sp}$ and $b \to b_{sp}$ where g_{sp} and b_{sp} are arbitrary setpoints selected to improve plasma stability. The above objective is reinterpreted in terms of impedance by noting that impedance is defined as the reciprocal of admittance, according to the following relationship:

$$z = \frac{1}{y} = r + jx = \frac{R + jX}{Z_0} = \frac{R + jX}{R_0 + j0} \qquad \text{EQN. 3}$$

where z is the normalized impedance, r and x are the resistance and reactance, respectively, $Z_0 = R_0 + j0$ denotes a nominal RF amplifier characteristic impedance. It follows that when $g \to 1$ and $b \to 0$, we obtain $R \to R_0$ and $X \to 0$.

[0071] Admittance regulation algorithm: The frequency control loop is designed by using conductance measurements, for example, as a PI control algorithm as follows:

$$f_{cmd} = -k_{pf}(g_{sp} - g) - k_{if} \int (g_{sp} - g)dt \qquad \text{EQN. 4}$$

where k_{pf} and k_{if} are scalar proportional and integral control gains. The shunt capacitance control loop is designed by using conductance measurements, for example, as a PI control algorithm as follows:

$$C_{tcmd} = -k_{pc}(b_{sp} - b) - k_{ic} \int (b_{sp} - b)dt \qquad \text{EQN. 5}$$

where k_{pc} and k_{ic} are scalar proportional and integral control gains.

[0072] In operation, referring now to Figs. 2, 3 and 6, after the user provides a non-zero setpoint, the trajectory generator and the power and admittance control algorithms are simultaneously activated and executed. The VI probe 240 provides analog signals proportional to the RF voltage and RF current, which are synchronously sampled by the

analog-to-digital converters, sent to a mixer and CIC filter (not shown) and ultimately sent through a calibration matrix to yield RF voltage and RF current measurements given by the following relationships:

$$\bar{V} = V_r + jV_i \text{ and } \bar{I} = I_r + jI_i \qquad \text{EQN. 6}$$

where $\bar{V}, \bar{I}$ denote vector representations of the instantaneous RF voltage and current, respectively, and subscripts r and i are used to denote the scalar values of the real and imaginary components.

[0073] The average delivered power is computed as follows:

$$P_{del} = \frac{1}{2}\mathrm{Re}\{\bar{V}\bar{I}^*\} = V_r I_r + V_i I_i \qquad \text{EQN. 7}$$

where $\mathrm{Re}\{\ \}$ denotes the real component of the vector, and superscript * is used to denote the complex conjugate of the vector.

[0074] The admittance vector $\bar{Y}$ is then computed as follows:

$$\bar{Y} = \frac{\bar{I}}{\bar{V}} = \frac{(I_r V_r + I_i V_i)}{V_r^2 + V_i^2} + j\frac{(I_i V_r - I_r V_i)}{V_r^2 + V_i^2} \equiv G + jB \qquad \text{EQN. 8}$$

where the conductance G and the susceptance B are real and imaginary components of the admittance $\bar{Y}$.

[0075] The normalized conductance g and normalized susceptance b are computed as follows:

$$g = Z_0 G = Z_0 \frac{(I_r V_r + I_i V_i)}{V_r^2 + V_i^2} \text{ and } b = Z_0 B = Z_0 \frac{(I_i V_r - I_r V_i)}{V_r^2 + V_i^2} \qquad \text{EQN. 9}$$

where Z_0 denotes the characteristic impedance of the RF amplifier. The measurements of P_{del}, g, b are respectively sent to the control algorithms for $P_{cmd}, f_{cmd}, C_{tcmd}$ respectively.

[0076] The electronic match controller 252 switches the FETs 256 (Fig. 6) thereby switching the shunt capacitors 258 to match the impedance between the power amplifier 220 and the dynamic load 260. The absence of moving mechanical parts leads to higher reliability. In one embodiment, the step response of the system 200 is faster than about 1 ms because the speed of the response is governed by the electronics and not by the mechanical response.

[0077] A change in frequency results in a change in both the conductance and the susceptance. However, for an integrated system without transmission line cables, a change in shunt capacitance results only in a change in the susceptance and does not affect the conductance value. Thus, the matrix that relates the controlled variable vector (formulated by the real and imaginary components of the admittance) and the controlling variable vector (formulated by the shunt and series capacitance or the shunt and frequency) is triangular. As a result, independent susceptance regulation is achieved by varying the shunt capacitance.

[0078] Independent susceptance regulation allows for the implementation of a frequency control algorithm based only on the deviation of the conductance from the conductance setpoint. As a result, both the conductance-based frequency control loop and the susceptance-based shunt capacitance control loop can be operated simultaneously and at high-speed, resulting in improved robustness.

[0079] Fig. 8 is a block diagram 300 of a method for determining the power dissipated (loss) in the electronic matching network 250 (Fig. 2) to improve the efficiency of the system 200. Step one (310), a power meter 314 (Fig. 9A) is calibrated into a 50 Ω calorimeter power reference to determine the power delivered to the 50 Ω load. Step two (320), a load simulator calorimeter 332 (Fig. 9B) is calibrated to a DC power reference to determine the power dissipated inside a load simulator 342 (Fig. 9D). Step three (330), the VI probe 240 (Fig. 2) is calibrated into a 50 Ω load to determine the power delivered by the power amplifier 220 (Fig. 2). Step four (340), the output of the system 200 is calibrated into the load simulator 342 to determine the power delivered to $Z_L = R_L + jX_L$. Step five (350), the power dissipated in the electronic matching system is calculated by difference between the he power delivered by the power amplifier 220 and the power delivered to $Z_L = R_L + jX_L$

[0080] Fig. 9A is detailed implementation diagram of step 310 for calibrating the power meter 314. A calorimeter 322 is coupled to the output of the VI Probe 240, RF power is applied from the power amplifier 220, and the power meter 314 is calibrated. Calorimetry is the measurement of thermal losses. It is implemented by thermally insulating the 50 Ω load in the calorimeter (322) to prevent ambient thermal losses and measuring the flow rate and the temperature rise of the cooling water. The power meter is calibrated to the power dissipation in the load computed by $Q = \frac{dm}{dt} C(T_{out} - T_{in})$,

where $\frac{dm}{dt}$ denotes the mass flow rate, C denotes the specific heat of water, and T_{in}, T_{out} denote the inlet and outlet temperatures, respectively. A computer 324 acquires flow rate and temperature measurements to compute the power dissipation in the load and the difference (error) with respect to readout of the power meter. The computer 324 then applies this error as a correction to the power meter to complete the calibration.

[0081] Fig. 9B is detailed implementation diagram of step 320 for calibrating the load simulator calorimeter 332. A load simulator calorimeter 332 is coupled to a DC power supply 334, DC power is applied, and the load simulator calorimeter 332 is calibrated. The DC power supply provides the DC power measurements. Using flow rate and temperature measurements at the inlet and outlet of the cooling system, a computer 324 computes the power dissipated in the load simulator. The computer 324 then applies the error between the power reported by the DC power supply and the power computed using calorimetry as a correction to the load simulator to complete the calibration.

[0082] Fig. 9C is detailed implementation diagram step 330 for calibrating an RF impedance analyzer or VI probe 240. Generally, the VI Probe 240 calibration in each integrated RF generator system 200 includes the following steps that yield a matrix transfer function that relates the VI probe voltage and current measured by the DSP compensator board 230 to an actual RF line voltage and current.

[0083] First, a short circuit connector 312 is coupled to the RF line output terminal of the VI probe 240, RF power is applied from the power amplifier 220, and Z_{sc}^{dsp} is computed, wherein Z_{sc}^{dsp} is defined as the ratio of V_{dsp} / I_{dsp} as measured by the DSP compensator board 230 for short circuit. Second, an open circuit connector 314 is coupled to the RF line output terminal of the VI probe 240, RF power is applied from the power amplifier 220, and Z_{oc}^{dsp} is computed, wherein Z_{oc}^{dsp} is defined as the ratio of V_{dsp} / I_{dsp} as measured by the DSP compensator board 230 for open circuit. Third, a 50 Ω load (Z_L) 316 is coupled to the output of the VI Probe 240, RF power is applied from the power amplifier 220, V_m and I_m are recorded and the RF line voltage V_L is computed, wherein $V_L = \sqrt{P_L Z_L}$. P_L is the delivered power measured by a power meter 318 at the 50 Ω load 316. Lastly, the VI probe calibration matrix transfer function is computed by the following equation:

$$\begin{bmatrix} \frac{V_L(t)}{I_L(t)} \end{bmatrix} = \begin{pmatrix} \frac{V_L}{V_m - Z_{sc}^{dsp} I_m} & \frac{-Z_{sc}^{dsp} V_L}{V_m - Z_{sc}^{dsp} I_m} \\ \frac{-V_L}{Z_L\left(-Z_{oc}^{dsp} I_m - V_m\right)} & \frac{Z_{oc}^{dsp} V_L}{Z_L\left(-Z_{oc}^{dsp} I_m - V_m\right)} \end{pmatrix} \begin{bmatrix} \frac{V_{dsp}(t)}{I_{dsp}(t)} \end{bmatrix} \quad \text{EQN. 10}$$

[0084] The expression in equation 10 translates VI probe measurement signals into RF line voltage and RF line current at the output of the VI probe 240.

[0085] Fig. 9D is detailed implementation diagram step 340 for calibrating the system 200 (Fig. 2). The system level calibration is used to quantify the power loss in the electronic matching network 250 for a range of values matching network variables. A load simulator 342 is coupled to the output of the electronic matching network 250. Typically, the load simulator is an electronic matching network inverse to the electronic matching network 250. A 50 Ω load is coupled to the output of the load simulator 342. The system-level calibration of the RF generator system 200 is performed as follows. First, a series inductance is adjusted in *ll* steps for $L_s \in \left[L_{s\min}, L_{s\max}\right]$. Second, a power setpoint value is changed in *pp* steps $P_{sp} \in \left[P_{sp\min}, P_{sp\max}\right]$ W. Third, a shunt capacitance setpoint value is changed in *cc* steps $C_{tcmd} \in \left[C_{tcmd\min}, C_{tcmd\max}\right]$. Lastly, an RF frequency value is changed in *ff* steps $f \in \left[f_{\min}, f_{\max}\right]$ Hz.

[0086] For each combination of the aforementioned steps, the load simulator 342 is set to present an impedance mismatch at the output of the electronic matching network 250. Next, RF power is applied from the power amplifier 220 and the power meter 314 measures the terminating load 312 resistance. The terminating load resistance is denoted by $P_{50\Omega}$ and transformed to the input of the load simulator 342. The simulated load is denoted by P_{sys} as $P_{sys} = f_{50\text{-}to\text{-}sim}(P_{50\Omega}, C_1, C_2)$, where C_1 and C_2 represent the series and shunt capacitance of the load simulator and $f_{50\text{-}to\text{-}sim}$ represents a tabular arrangement. The losses associated in electronic matching network 250 is computed by the difference between the P_L and $P_{50\Omega}$.

[0087] In some embodiments, a calibration table which has dimensions $ll \times pp \times cc \times ff$ can stored in non-volatile memory (e.g., flash memory) as $P_{sys} = f_{VI\text{-}to\text{-}sim}(L_s, P_{sp}, C_{tcmd}, f)$, where $f_{VI\text{-}to\text{-}sim}$ represents a tabular arrangement. High-speed real-time control loops

necessitate fast searches through the calibration table during operation of the system 200. Non-volatile memory (e.g., flash memory) tends to be slower than the volatile memory (e.g., Dynamic RAM). The high-speed volatile memory is effectively utilized, wherein the arrangement of the calibration table (dimensions $ll \times pp \times cc \times ff$) can be based on how frequently L_s, P_{sp}, C_{tcmd}, and f are changed. Specifically, the calibration table can be segmented into ll memory blocks; each block including pp memory pages; each memory page including a $cc \times ff$ dimensional table. A new memory block can be loaded into non-volatile memory when L_s is changed, a new memory page can be loaded when power setpoint is changed, and calibration points for the appropriate memory page associated with C_{tcmd} and f can be executed in real-time.

[0088] Fig. 11 is a diagram of an RF power delivery system 1105 that provides synchronous power to one or more loads, 1140a, 1140b...1140n, generally 1140. The RF power delivery system 1105 includes a master RF power delivery system 1110, and one or more slave RF power delivery systems, 1120a, 1120b...1120n, generally 1120. In contrast to the fraction of the total rated power delivered to each individual load by the RF power delivery system 140 (FIG. 1D), the RF power delivery system 1105 delivers the total rated power of a single RF power delivery system into each individual load 1140. The RF power delivery system 1105 delivers the total rated power to each individual load 1140 using the master RF power delivery system 1110 to supply the first load 1140a and one or more slave power delivery systems 1120 to supply one or more additional loads 1140. To this end, the master RF power delivery system 1110 sets one or more slave RF power delivery systems 1120 to a frequency f and a phase ϕ equal to its own frequency and phase ϕ as will be discussed below with reference to FIGS. 12, 13A, and 13B.

[0089] FIG. 12 shows an embodiment of an RF power delivery system 1105 that provides power to one or more loads 1140, while allowing for phase compensation. The RF power delivery system 1105 includes a master RF power delivery system 1110 and one or more slave RF power delivery systems 1120. The master RF power delivery system 1110 and each slave RF power delivery system 1120 includes a DC source 1250, a RF power amplifier 1210, a VI Probe 1220, and an electronic matching system 1240. The DC source 1250 provides power to the RF power amplifier 1210. The VI probe 1220 adjusts the set point of the DC source 1250 and adjusts the shunt capacitance of the electronic matching system 1240. The electronic matching system 1240 switches shunt capacitors

(not shown) to match the impedance between the RF power amplifier 1210 and the load 1140 to facilitate stable and maximum power transfer from the RF power amplifier 1210 to the load 1140.

[0090] The RF power amplifier 1210 converts the DC power from the DC source 1250 to an RF power at a frequency. Since the RF power amplifier 1210 introduces an arbitrary phase shift it is necessary to adjust the phase of the RF power amplifier 1210 to ensure the power delivered to one or more loads 1140 is synchronous. To ensure the arbitrary phase shift does not prevent the phase of the RF power amplifier 1210 output to be regulated to a commanded phase set point, the RF power amplifier 1210 has phase compensation, as will be discussed below with reference to FIG. 12A. The commanded phase set point can be driven by, for example, a Direct Digital Synthesizer (DDS) 1230. Further, if an RF amplifier is driven by a pulse train with frequency f and a phase ϕ, the output of the RF amplifier will retain the frequency f but may introduce a phase shift of $\Delta\phi$ resulting in a total phase of $\phi+\Delta\phi$. For example, assume a pulse train having phase $\phi = 0$, a master RF power delivery system 1110 and one slave RF power delivery system 1120a having an in-phase configuration an no phase adjusting circuit. The total power delivered is defined by the following equation:

$$\begin{aligned} p(t) &= p_1(t) + p_2(t) \\ &= P_0 \cos(2\pi ft + (\phi + \Delta\phi_1)) + P_0 \cos(2\pi ft + (\phi + \Delta\phi_2)) \quad , \end{aligned} \qquad \text{EQN. 11}$$

where $p_1(t)$ and $p_2(t)$ denote power delivered by the master RF power delivery system 1110 and the slave power delivery system 1120a respectively. P_0 denotes the constant peak delivered power and f denotes the frequency. If the master RF power delivery system 1110 introduces an arbitrary phase shift of $\Delta\phi_1 = 0$ and the slave RF power delivery system 1120a introduces an arbitrary phase shift of $\Delta\phi_2 = \pi = 180^\circ$, then the output power is zero, as shown by the following equation:

$$\begin{aligned} p(t) &= p_1(t) + p_2(t) \\ &= P_0 \cos(2\pi ft + 0) + P_0 \cos(2\pi ft + \pi) \\ &= P_0 \cos(2\pi ft) - P_0 \cos(2\pi ft) = 0 \, . \end{aligned} \qquad \text{EQN. 12}$$

It then follows that any non-zero value of $\Delta\phi_2$ proportionally reduces the output power.

[0091] FIG. 12A shows a detailed embodiment of a master-slave RF power amplifier 1210 including phase compensation. The master-slave power amplifier 1210 includes a

phase compensator circuit 1215, an RF power amplifier 1225, and a phase detector 1235. The phase detector 1235 detects the phase of the RF power amplifier 1225. The detected phase is input to the phase compensator circuit 1215. The phase compensator circuit 1215 compares the phase detected by the phase detector 1235 to the phase set point (ϕ_{sp}) that is input from the DSP board (not shown). The phase compensator circuit 1215 adjusts the RF power amplifier's 1225 phase to compensate for an arbitrary phase shift ($\Delta\phi_1$) introduced by the RF power amplifier 1225.

[0092] FIG. 13A shows one embodiment of an in-phase configuration of an RF power delivery system 1105. The RF power delivery system 1105 includes a master RF power delivery system 1110 that sets the frequency of a slave RF power delivery system 1120 each of which drive a primary side of a transformer 1330. The transformer 1330 is configured for an in-phase configuration of the master RF power delivery system 1110 and the slave power delivery system 1120. For an in-phase configuration if the arbitrary phase shift for the master RF power delivery system 1110 is $\Delta\phi_1 = 0$ then the desired arbitrary phase shift for the slave RF power delivery system 1120 is $\Delta\phi_2 = 0$ to obtain a total power shown by the following equation:

$$\begin{aligned} p(t) &= p_1(t) + p_2(t) \\ &= P_0 \cos(2\pi ft + 0) + P_0 \cos(2\pi ft + 0) \\ &= 2 \cdot P_0 \cos(2\pi ft) \ . \end{aligned} \qquad \text{EQN. 13}$$

[0093] FIG. 13B shows one embodiment of an out-of-phase configuration of an RF power delivery system 1105. The RF power delivery system 1105 includes a master RF power delivery system 1110 that sets the frequency of a slave RF power delivery system 1120 each of which drive a primary side of a transformer 1330. The transformer 1330 is configured for an out-of-phase configuration of the master RF power delivery system 1110 and the slave power delivery system 1120. For an out-of-phase configuration if the arbitrary phase shift for the master RF power delivery system 1110 is $\Delta\phi_1 = 0$ then the desired arbitrary phase shift for the slave RF power delivery system 1120 is $\Delta\phi_2 = \pi = 180^\circ$ to obtain a total power of:

$$\begin{aligned} p(t) &= p_1(t) - p_2(t) \\ &= P_0 \cos(2\pi ft + 0) - P_0 \cos(2\pi ft + \pi) \\ &= P_0 \cos(2\pi ft) + P_0 \cos(2\pi ft) \\ &= 2 \cdot P_0 \cos(2\pi ft) \ . \end{aligned}$$ EQN. 14

[0094] FIG. 14 is one embodiment of an analog-digital hybrid control loop for a power converter system 1400. The power converter system 1400 includes a power converter 1405, an analog control loop 1415, and a digital control loop 1430. A power converter 1405 includes a Fast DC Bus 210 (FIG. 2), Fast Bus Controller 212 (FIG. 2), PA Gate Drive 222 (FIG. 2), and a RF Power Amplifier 220 (FIG.2). The digital control loop 1430 includes an analog-to-digital converter 1410, a digital control 1430, and a digital-to-analog converter 1425. The analog-to-digital converter 1410 digitizes an analog measurement measured at the power converter 1405. The digitized measurement and a digital set point are input to a digital control 1430 that outputs a digital power converter set point. The digital power converter set point is converted by the digital-to-analog converter 1425 to an analog power converter set point. The analog power converter set point is input to the analog control loop. The analog control loop includes an analog control 1415 and a output conditioning block 1420. The analog control 1415 uses an analog measurement from the power converter 1405 and the analog set point from the digital control loop to generate an analog output to input to the output conditioning block 1420. The output conditioning block generates an output to regulate the power converter 1405.

[0095] FIG. 15 is one embodiment of an On Chamber RF power delivery system 1500 including the analog-digital hybrid control loop, as described above with reference to FIG. 14. The On Chamber RF power delivery system 1500 includes an RF amplifier 1505, a Fast Bus 1510, an analog-to-digital converter 1515, a controller 1520, a digital-to-analog converter 1525, an analog compensation network 1530, and a output conditioning 1540. The RF amplifier 1505 delivers RF power to an RF load 1545 (e.g., an inductively-coupled plasma in a chamber driven by a coil). The input to the RF amplifier 1505 is a DC power supplied by the Fast Bus 1510. The input to the Fast Bus 1510 is a Pulse Width Modulated (PWM) signal that is generated by the analog-digital hybrid control

loop. The analog-digital hybrid control loop consists of two controls loops, a digital control loop 1430 and an analog control loop 1415.

[0096] The digital control loop operates by converting a measurement of the power delivered by the RF Amplifier 1510 to a digital delivered power value (P_{del}) using an analog-to-digital converter 1515. The digital delivered power value (P_{del}) is input to a controller 1540 that also has input RF power set point (P_{sp}) that is provided to the controller 1520 by the user. The controller 1520 generates a current set point (I_{ref}) that is applied to the analog control loop, as discussed further below. The current set point (I_{ref}) is a function of the digital delivered power value (P_{del}) and the RF power set point (P_{sp}), $I_{ref} = f(P_{sp}, P_{del})$, where f is a known function. In its simplest form f is a form of a proportional-integral (PI) control as shown by the following equation:

$$I_{ref} = k_p (P_{sp} - P_{del}) + k_i \int_0^t (P_{sp} - P_{del})\, d\tau \,, \qquad \text{EQN. 15}$$

where k_p and k_i are positive scalar gains for the proportional and integral components respectively. In some embodiments, f may be model-based or empirically determined.

[0097] The analog control loop 1415 has an analog compensation network 1530 with DC current measurement (I_{dc}) and current set point (I_{ref}) as inputs. The analog compensation network 1530 uses I_{dc} to generate a duty cycle command V_{duty}. The duty cycle command V_{duty} is used as input to the output conditioning block 1540. The output conditioning block 1535 generates a PWM signal that regulates the input to the RF amplifier 1505 when input to the Fast Bus 1510.

[0098] In some embodiments, the controller 1545 can be a Digital Signal Processor (DSP), a Field Programmable Gate Array and/or a microcontroller.

[0099] FIG. 16 is a circuit diagram of a compensation network 1550. The compensation network 1550 is based on an Average Current Control technique that is described, for example, in *"Average Current Mode Control of Switching Power Supplies," U-140, Unitrode Application Note, Texas Instruments by Lloyd Dixon*, the entirety of which is incorporated herein by reference. The compensation network 1550 resistors, R_f 1630 and R_i 1620, and capacitors, C_p 1605 and C_z 1615, are selected with values to satisfy the desired poles and zeros. The desired poles and zeros are selected to achieve the maximum phase margin and gain-bandwidth product. The zero is located at R_fC_z and the poles are located at 0 and $R_fC_pC_z/(C_p + C_z)$ as is shown by the transfer function below:

$$H(s) = \frac{R_f C_z s + 1}{s\left[R_f C_p C_z s + (C_p + C_z)\right]} \qquad \text{EQN. 16}$$

where s denotes the Laplace transform. Additionally, the pulse width modulation signal generated by output conditioning block 1540 (FIG. 15) has a gain at the switching frequency that is determined by the ratio of R_f/R_i.

While this invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

CLAIMS

1. A hybrid system for delivering power to a load, comprising;

a power converter system;

an outer loop coupled to the power converter system that provides a gain-bandwidth and a phase margin for substantially maintaining stability of output power; and

an inner loop coupled to the power converter system for compensating for nonlinearities in the power converter system.

2. The system of claim 1, wherein the outer loop is an analog control loop.

3. The system of claim 2, wherein the inner loop is a digital control loop.

4. The system of claim 3, wherein the analog control loop includes an analog control, and an output conditioning block for regulating output power.

5. The system of claim 4, wherein the digital control loop includes:

an analog-to-digital converter for converting an analog measurement taken at the power converter to a digital measurement for determining a digital current set point;

a digital control to output the digital current set point for determining a power width modulation signal; and

a digital-to-analog converter for converting the digital current set point to an analog current set point for determining the power width modulation signal for regulating output power.

6. The system of claim 5, wherein the analog control loop outputs the power width modulated signal based on the analog current set point and an analog measurement taken at the power converter system for regulating output power.

7. The system of claim 5, wherein the power converter system includes a DC source, and a RF power amplifier.

8. The system of claim 7, wherein a RF power measurement taken at the RF power amplifier is digitized by the analog-to-digital converter to produce a digital RF power measurement for determining a pulse width modulation signal for regulating output power.

9. The system of claim 8, wherein the digital control outputs a digital current set point for determining the pulse width modulation signal for regulating output power.

10. The system of claim 9, wherein the digital current set point is converted to a analog current set point for determining the pulse width modulation signal for regulating output power.

11. The system of claim 10, wherein the analog control loop outputs the power width modulated signal based on the analog current set point and an analog current set point measurement taken at the DC source for regulating output power.

12. A digital and analog hybrid method for delivering power to a load, comprising:

providing a gain-bandwidth and a phase margin for substantially maintaining stability of an output power; and

compensating for nonlinearities in the in the output power.

13. The method of claim 12, further comprising:

measuring delivered RF power signal;

converting the measured delivered RF power from an analog signal to a digital delivered RF power signal; and

determining a digital current set point from the digital delivered RF power signal and a RF power set point.

14. The method of claim 13, further comprising:

converting the digital current set point from a digital signal to an analog current set point signal;

measuring DC current at a power supply; and

determining a duty cycle command from the analog current set point signal and the DC current.

15. The method of claim 14, further comprising:

determining a pulse width modulation signal from the duty cycle command; and

regulating the power supply with the pulse width modulation signal.

16. A system for delivering synchronous power, comprising:

a master power system having a maximum power that delivers power to a first dynamic load; and

a slave power system having a maximum power equal to the maximum power of the master power system and delivers power having a phase equal to a phase supplied by the master power system to a second dynamic load.

17. The system of claim 16, wherein the master power system includes:

a DC source for supplying power;

a RF power amplifier with phase compensation for supplying power with a substantially constant phase;

a VI probe for monitoring the phase of the RF power amplifier output; and

an electronic matching system for matching the phase of the RF power amplifier and the load.

18. The system of claim 17, wherein the output the master power system delivers to the load depends on the output of the VI probe.

19. The system of claim 16, wherein the RF power amplifier with phase compensation includes:

a phase compensator circuit for supplying a phase command to a RF power amplifier to compensate for an arbitrary phase shift; and

a phase detector for detecting the phase of the output power.

20. The system of claim 14, wherein the slave power system includes:

a DC source for supplying power;

a RF power amplifier with phase compensation for supplying power with a substantially constant phase;

a VI probe for monitoring the phase of the RF power amplifier output; and

an electronic matching system for matching the phase of the RF power amplifier and the load.

21. The system of either claim 19, wherein the RF power amplifier with phase compensation includes:

a phase compensator circuit for supplying a phase command to a RF power amplifier to compensate for an arbitrary phase shift; and

a phase detector for detecting the phase of the output power.

22. The system of claim 14, wherein the master power system is 180 degrees out of phase with the slave power system.

23. The system of claim 14, wherein the master power system controls two or more slave power systems to deliver power with an amplitude and phase equal to the amplitude and phase of the master power system to two or more loads.

24. A method for delivering synchronous power , comprising:

delivering power and phase to a first load; and

delivering power and phase substantially equal to the power and phase delivered to the first load to a second load.

25. The method of claim 24, further comprising:

compensating for an arbitrary phase shift in the phase of the output to the first load; and

substantially maintaining the phase of the output to the first load.

26. The method of claim 24, further comprising:

compensating for an arbitrary phase shift in the phase of the output to the second load; and

substantially maintaining the phase of the output to the second load.

27. The method of claim 24, further comprising delivering power with an amplitude and phase equal to the amplitude and phase of the first load to one or more loads.

28. A digital and analog hybrid system for delivering power to a load, comprising:

means for providing a gain-bandwidth and a phase margin for substantially maintaining stability of output power; and

means for compensating for nonlinearities at the load.

29. A system for delivering synchronous power, comprising:

means for delivering power to a first dynamic load; and

means delivering power having a phase equal to phase of the first dynamic load to a second dynamic load.

30. A method for delivering power to a dynamic plasma load, comprising:

determining a switch of reactant gases that generate a plasma;

calculating a change in output power required to sustain a plasma load with the switched reactant gases;

supplying power equal to a power required to sustain the plasma load with the switched reactant gases; and

supplying power to the plasma load faster than the reactant gases change in the plasma .