ABSTRACT OF THE DISCLOSURE

An electrode structure as well as the fabrication method thereof is disclosed which may enable successful pad layout conversion of interconnection electrode pads on the periphery of an associated IC chip to a grid array of rows and columns of terminal solder pads arranged occupying the entire area of the opposite surface of the chip while permitting use of a minimized length of wire leads for interconnection therebetween. This is achieved by (i) preparing a flat square IC chip which has an array of regularly spaced peripheral bonding pads the number of which along each of four chip sides is equally defined by a function of 2i(2i - 1) where "i" is an integer and which also has external connection pads made of aluminum, (ii) sequentially forming nickel and gold coat films on the chip by electroless plating techniques, (iii) electrically coupling by metal contacts using thermal compression-bonding techniques the peripheral bonding pads to the pad layout conversion substrate for rearrangement of the peripheral bonding pads into the grid array of solder pads, and (iv) filling an adhesion resin between the conversion substrate and the IC chip.

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