CLAIMS

1. A method for migrating memory data, wherein a hybrid memory system comprises a plurality of processors and a plurality of memory media of different types, and the processor is associated with at least two memory media of different types; and the method comprises:

sampling a plurality of memory channels in a computer device according to a sampling strategy, and determining access frequencies of interleaved data blocks in sampled memory channels, wherein the plurality of memory channels allow a processor in the computer device to access the memory media in an interleaving manner, and the sampling strategy indicates a rule for sampling memory channels based on a space dimension and a time dimension;

determining, based on the access frequencies of the interleaved data blocks, access frequencies of pages in which the interleaved data blocks are located in the memory media, wherein the access frequencies of the pages in which the interleaved data blocks are located are used to determine access temperatures of the pages; and

triggering data migration between the at least two memory media of different types based on the access temperatures.

2. The method according to claim 1, wherein sampling the plurality of memory channels in the computer device according to the sampling strategy comprises:

sampling the plurality of memory channels based on page identifiers indicated by the sampling strategy and spatial distribution of the memory channels, to obtain the sampled memory channels.

3. The method according to claim 2, wherein sampling the plurality of memory channels based on the page identifiers indicated by the sampling strategy and the spatial distribution of the memory channels, to obtain the sampled memory channels comprises:

sampling the plurality of memory channels based on a correspondence between the page identifiers and the memory channels, to obtain the sampled memory channels.

4. The method according to any one of claims 1 to 3, wherein sampling the plurality of memory channels in the computer device according to the sampling strategy comprises:

sampling the plurality of memory channels in a rotational sampling manner indicated by the sampling strategy, to obtain the sampled memory channels, wherein the rotational sampling manner indicates a change manner of a correspondence between a page identifier and a memory channel.

5. The method according to any one of claims 1 to 3, wherein sampling the plurality of memory channels in the computer device according to the sampling strategy comprises:

sampling the plurality of memory channels based on a correspondence between a time period

indicated by the sampling strategy and storage space of the memory medium, to obtain the sampled memory channels.

6. The method according to claim 5, wherein sampling the plurality of memory channels in the computer device according to the sampling strategy comprises:

sampling the plurality of memory channels in a rotational sampling manner indicated by the sampling strategy, to obtain the sampled memory channels, wherein the rotational sampling manner indicates a change manner of the correspondence between the time period and the storage space of the memory medium.

7. The method according to any one of claims 1 to 6, wherein sampling the plurality of memory channels in the computer device according to the sampling strategy comprises:

sampling, according to the sampling strategy, a plurality of memory channels corresponding to addresses indicated by access requests, wherein the access request indicates an operation performed by an application run by the processor in the computer device on the memory medium.

8. The method according to any one of claims 1 to 7, wherein a size of the interleaved data block is a multiple of a size of a cache line of accessing the memory medium by the processor.

9. An apparatus for migrating memory data, comprising:

a sampling module, configured to sample a plurality of memory channels in a computer device according to a sampling strategy, wherein the plurality of memory channels allow a processor in the computer device to access memory media in an interleaving manner, and the sampling strategy indicates a rule for sampling memory channels based on a space dimension and a time dimension;

a statistics collection module, configured to determine access frequencies of interleaved data blocks in sampled memory channels, wherein

the statistics collection module is further configured to determine, based on the access frequencies of the interleaved data blocks, access frequencies of pages in which the interleaved data blocks are located in the memory media, wherein the access frequencies of the pages in which the interleaved data blocks are located are used to determine access temperatures of the pages; and

a migration module, configured to trigger data migration between at least two memory media of different types based on the access temperatures.

10. The apparatus according to claim 9, wherein when sampling the plurality of memory channels in the computer device according to the sampling strategy, the sampling module is specifically configured to:

sample the plurality of memory channels based on page identifiers indicated by the sampling strategy and spatial distribution of the memory channels, to obtain the sampled memory channels.

11. The apparatus according to claim 10, wherein when sampling the plurality of memory

channels based on the page identifiers indicated by the sampling strategy and the spatial distribution of the memory channels, to obtain the sampled memory channels, the sampling module is specifically configured to:

sample the plurality of memory channels based on a correspondence between the page identifiers and the memory channels, to obtain the sampled memory channels.

12. The apparatus according to any one of claims 9 to 11, wherein when sampling the plurality of memory channels in the computer device according to the sampling strategy, the sampling module is specifically configured to:

sample the plurality of memory channels in a rotational sampling manner indicated by the sampling strategy, to obtain the sampled memory channels, wherein the rotational sampling manner indicates a change manner of a correspondence between a page identifier and a memory channel.

13. The apparatus according to any one of claims 9 to 11, wherein when sampling the plurality of memory channels in the computer device according to the sampling strategy, the sampling module is specifically configured to:

sample the plurality of memory channels based on a correspondence between a time period indicated by the sampling strategy and storage space of the memory medium, to obtain the sampled memory channels.

14. The apparatus according to claim 13, wherein when sampling the plurality of memory channels in the computer device according to the sampling strategy, the sampling module is specifically configured to:

sample the plurality of memory channels in a rotational sampling manner indicated by the sampling strategy, to obtain the sampled memory channels, wherein the rotational sampling manner indicates a change manner of the correspondence between the time period and the storage space of the memory medium.

15. The apparatus according to any one of claims 9 to 14, wherein when sampling the plurality of memory channels in the computer device according to the sampling strategy, the sampling module is specifically configured to:

sample, according to the sampling strategy, a plurality of memory channels corresponding to addresses indicated by access requests, wherein the access request indicates an operation performed by an application run by the processor in the computer device on the memory medium.

16. The apparatus according to claim 9, wherein a size of the interleaved data block is a multiple of a size of a cache line of accessing the memory medium by the processor.

17. A memory, wherein the memory comprises a storage medium and a controller, and the storage medium is configured to store a group of computer instructions; and when executing the

group of computer instructions, the controller performs an operation step of the method according to any one of claims 1 to 8, to identify an access frequency at which a data block in the memory is accessed by an application.

18. A chip, comprising a processor and a power supply circuit, wherein the power supply circuit is configured to supply power to the processor; and the processor is configured to perform an operation step of the method according to any one of claims 1 to 8, to identify an access frequency at which a data block in a memory is accessed by an application.

19. A processor, wherein the processor is associated with at least two memory media of different types, and the processor is configured to perform an operation step of the method according to any one of claims 1 to 8, to identify an access frequency at which a data block in the memory media is accessed by an application.

20. A computer device, wherein the computer device comprises a storage, a processor, and a plurality of memory media of different types, the processor is associated with at least two memory media of different types, the storage is configured to store a group of computer instructions, and when executing the group of computer instructions, the processor performs an operation step of the method according to any one of claims 1 to 8, to identify an access frequency at which a data block in the memory media is accessed by an application.