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(54) Title: CROSS FIELD EFFECT TRANSISTOR LIBRARY CELL ARCHITECTURE DESIGN

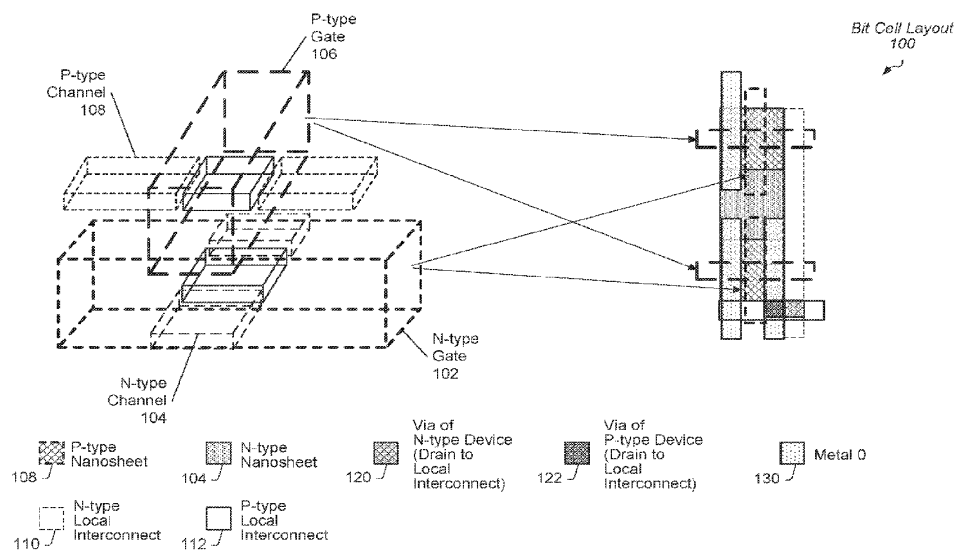


FIG. 1

(57) Abstract: A system and method for efficiently creating layout for memory bit cells are described. In various implementations, cells of a library use Cross field effect transistors (FETs) that include vertically stacked gate all around (GAA) transistors with conducting channels oriented in an orthogonal direction between them. The channels of the vertically stacked transistors use opposite doping polarities. A first category of cells includes devices where each of the two devices in a particular vertical stack receive a same input signal. The second category of cells includes devices where the two devices in a particular vertical stack receive different input signals. The cells of the second category have a larger height dimension than the cells of the first category.

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