

**WIRELESS SYNCHRONOUS CLOCK SYSTEM****FIELD OF THE INVENTION**

5           The present invention relates generally to master/slave clock systems for synchronizing the time for plurality of clocks, and in particular, to a wireless synchronous clock system which can also function as a public address system.

10                           **BACKGROUND OF THE INVENTION**

          The master/slave clock systems are generally well known. They are commonly used in a facility where multiple clocks which are separated by some distance need to be synchronized at all times. For instance, such a  
15   system is used in a college campus setting where many clocks are spread out throughout the campus area. Rather than adjusting the time on each clock individually, a master/slave system allows all clocks, or the slave clocks, to be updated by simply controlling a single clock, or the master clock.

20           To have a proper master/slave clock system, there must be a way to communicate between the master clock and the slave clocks. Traditionally, this was done via a cable connection. Such a system is cumbersome in that the slave clocks cannot be easily relocated since a new cable connection must be created. Moreover, cable connection is expensive and  
25   labor intensive to implement. Furthermore, cable system is not optimally adapted to be used also as public announcement system due to the

difference in the voltage requirements between the clock and the announcement systems. Therefore, it would be highly desirable to have wireless master/slave synchronous clock system which is convenient and versatile, and which can be easily and cost effectively implemented.

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### OBJECT OF THE INVENTION

Therefore, it is an object of the present invention to have a wireless master/slave synchronous clock system which can be easily and cost  
10 effectively implemented.

It is another object of the present invention to have a wireless master/slave synchronous clock system which is convenient to use.

It is yet another object of the present invention to have a wireless master/slave synchronous clock system which can be also function as a  
15 zonable public address system with zonable message board capability.

### SUMMARY OF THE INVENTION

The present system basically comprises two sets of circuitry, one at  
20 the master clock side, or the base station, and one the slave clock side, or the terminal. In a typical setting, one base station controls a plurality of clocks at the terminals which are spread out over a distance.

The base station circuit includes an external VHF/UHF antenna, a base station PC, baseband processor, and an external antenna. The base  
25 station PC includes a reference time extractor, RS 232 serial port, system control software, and user input devices such as a keyboard and a mouse.

The VHF/UHF antenna is used to receive a standard TV signal which commonly carries a time signal in the teletext. The teletext is received by the reference time extractor which extracts the time signal. The extracted time is used as the reference time for all the clocks. The system control  
5 software controls all of the system processes which will be discussed below.

The baseband processor includes an embedded microcontroller; watchdog; quartz real time clock (RTC); audio amplifier; FFSK (fast frequency shift key) modulator; RS 232 interface; optionally, a parallel port;  
10 simplex RF transmitter; and a microphone.

When a TV signal is received by the reference time extractor, it extracts the reference time signal. This reference time signal is used to first update the PC's own internal clock which is commonly found in all PCs. A time signal is then generated from the PC's internal clock. This time signal  
15 from the PC's internal clock is then sent to the embedded microcontroller via the RS 232 serial interface. This time signal is then first used to update the RTC 36 of the baseband processor and is then sent to the FFSK modulator which converts the digital signal to an analog signal suitable for RF transmission. The analog time signal is then sent to the simplex RF  
20 transmitter which modulates the signal onto a RF carrier frequency. The RF signal is then transmitted via the external antenna to each of the terminals.

To ensure a smooth running of the base station, several safeguards have been implemented. For instance, when a reference time signal becomes unavailable for some reason, a time signal is still available  
25 through the PC's own internal clock. If for some reason, the base station PC is disconnected from the baseband processor, then the RTC is used to

generate the reference time signal. In the event that the microcontroller hangs, the watchdog resets it.

The circuitry at the terminal includes an antenna; simplex RF receiver; quartz real time clock (RTC); watchdog; FFSK demodulator; display; custom display driver; a microcontroller; message display board; RS 232 serial interface; an audio amplifier; and a speaker.

The RF signal containing the time information from the base station is received by the antenna which is demodulated by the receiver. The demodulated signal is then converted to a digital signal by the FFSK demodulator. The digital time signal is then sent to the microcontroller. The digital time signal is used to update the RTC. The time signal from the RTC is used to display the time on the display. Here, a 7-segment display is used, though other types of displays are clearly possible. The custom display driver is used to control the display. Like in the baseband processor, the terminal includes the watchdog which resets the microcontroller in the event it hangs.

Because the time updating process will generally take up a very short amount of time each day, the system can easily double up as a public address (PA) system with optional message board capability. To facilitate the PA functionality, a microphone and audio amplifier are provided. A switch connects to the amplifier when the PA feature is in use. The switch connects back to the FFSK modulator when the system is being used to update the clocks, when the base station is instructing the clock terminals to go into the PA mode, or when a text message for the message board is being transmitted. From the terminal side, an audio amplifier and a speaker are provided. When a person speaks into the microphone, the

audio signal is amplified by the amplifier and sent directly to the RF transmitter to be transmitted. The audio signal is received by the RF receiver at the terminal side. The audio is amplified further by the amplifier and sent to the speaker.

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### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of the circuitry employed at the base station in the present wireless synchronous clock system.

10        FIG. 2 is a schematic diagram of the circuitry employed at the terminals in the present wireless synchronous clock system.

### DETAILED DESCRIPTION OF THE INVENTION

15        The present system basically comprises two sets of circuitry, one at the master clock side, or the base station, and one the slave clock side, or the terminal. In a typical setting, one base station controls a plurality of clocks at the terminals which are spread out over a distance. The schematic diagram of the circuitry at the base station 1 is illustrated in FIG. 1 and the schematic diagram of the circuitry at the terminal 2 is illustrated in FIG. 2.

20        Referring first to FIG. 1, the base station circuit 1 includes an external VHF/UHF antenna 5, a base station PC 10, baseband processor 30, and an external antenna 50. The base station PC includes a reference time  
25        extractor 12, RS 232 serial port 14, system control software 16, and user input devices such as a keyboard 18 and a mouse 19. The VHF/UHF

antenna 5 is used to receive the standard TV signal which commonly carries a time signal in the teletext. The VHF/UHF antenna 5 can also receive GPS signal which provides precise time information. The teletext is received by the reference time extractor 12 which extracts the time  
5 signal. The extracted time is used as the reference time for all the clocks. The system control software 16 controls all of the system processes which will be discussed below. All data communicated between the base station PC 10 and the baseband processor 30 is done via the RS 232 serial port 14.

10 Still referring to FIG. 1, the baseband processor 30 includes an embedded microcontroller 32; watchdog 34; quartz real time clock (RTC) 36; audio amplifier 38; FFSK (fast frequency shift key) modulator 40; RS 232 interface 42; optionally, a parallel port 44; simplex RF transmitter 46; and a microphone 48. Although the preferred arrangement of the base  
15 station 1 is to have a separate base station PC 10 and a baseband processor 30, it is possible to combine them into a single unit where only a single processor is employed.

When a TV signal is received by the reference time extractor 12, it extracts the reference time signal. This reference time signal is used to first  
20 update the PC's own internal clock which is commonly found in all PCs. A time signal is then generated from the PC's internal clock. This time signal from the PC's internal clock is then sent to the embedded microcontroller 32 via the RS 232 serial interface 42. This time signal is then first used to update the RTC 36 of the baseband processor, and is then sent to the  
25 FFSK modulator 40 which converts the digital time signal to an analog signal suitable for RF transmission. The analog time signal is then sent to

the simplex RF transmitter 46 which modulates the signal onto a RF carrier frequency. The RF signal is then transmitted via the external antenna 50 to each of the terminals.

To ensure a smooth running of the base station, several safeguards  
5 have been implemented. For instance, when a reference time signal becomes unavailable for some reason, a time signal is still available through the PC's own internal clock. If for some reason, the base station PC is disconnected from the baseband processor 30, then the RTC 36 is used to generate the reference time signal. In the event that the  
10 microcontroller 32 hangs, the watchdog 34 resets it.

Now referring to FIG. 2, the circuitry at the terminal 2 includes an antenna 60; simplex RF receiver 62; quartz real time clock (RTC) 64; watchdog 66; FFSK demodulator 68; display 70; custom display driver 72; a microcontroller 74; message display board 76; RS 232 serial interface  
15 78; an audio amplifier 80; and a speaker 82.

Still referring to FIG. 2, the RF signal containing the time information from the base station 1 is received by the antenna 60 which is demodulated by the receiver 62. The demodulated signal is then converted to a digital signal by the FFSK demodulator 68. The digital time  
20 signal is then sent to the microcontroller 74. The digital time signal is used to update the RTC 64. The time from the RTC 64 is used to display the time on the display 70. Here, a 7-segment display is used, though other types of displays are clearly possible. The custom display driver 72 is used to control the display. Like in the baseband processor 30, the terminal 2  
25 includes the watchdog 66 which resets the microcontroller 74 in the event it hangs.

How frequently the system is updated with the reference time signal is up to the user. A time-update frequency parameter and data-integrity parameter can be programmed into the system control software 16 such that a user could input the time-update frequency and data-integrity parameter via the keyboard 18 or the mouse 19. Given the relatively high accuracy of quartz clocks, an update once a day or once every other day would be sufficient for most purposes.

Because the time updating process will generally take up a very short amount of time each day, the system can easily double up as a public address (PA) system with optional message board capability. To facilitate the PA functionality, the microphone 48 and audio amplifier 38 are provided, as shown in FIG. 1. A switch 39 connects to the amplifier 38 when the PA feature is in use. The switch 39 connects back to the FFSK modulator 40 when the system is being used to update the clocks, when the base station is instructing the clock terminals to go into the PA mode, or when a text message for the message board 76 is being transmitted. From the terminal side, FIG. 2, an audio amplifier 80 and a speaker 82 are provided. When a person speaks into the microphone 48, the audio signal is amplified by the amplifier 38 and sent directly to the RF transmitter 46 to be transmitted. The audio signal is received by the RF receiver 62 at the terminal side. The audio is amplified further by the amplifier 80 and sent to the speaker 82.

To display a message on the message display board 76, a user simply types in a message on the keyboard 18. The message signal is sent to the baseband processor via the RS 232 interface and is processed in a manner identical to the reference time signal. The message signal is

processed in a manner similar to the reference time signal from the terminal side as well, except that when it reaches the microcontroller 74, the message signal is sent to the message display board 76 via the RS 232 interface 78 instead of the display 70.

5           To give versatility to the system, a header is provided for both the reference time signal, text message signal, and the audio signal by the microcontroller 32. The header contains information about the signal such as whether it is a time, data, or audio signal so that the microcontroller 74 can determine the correct course of action and the proper destinations for  
10       the signals it receives.

          To have individual control over each of the terminals, an address is provided for each terminal. An address can be included in the header of a signal such that only the selected terminals are affected. For instance, if a public announcement only needs to be made in a few selected areas, the  
15       appropriate address can be indicated in the header. For the terminals not selected, the microcontroller 74 prevents the audio from reaching the speaker.

          Although the header can come in a number of different format, the present invention employs a 6-byte header. The first byte is the system ID  
20       which allows different network of the present wireless system to co-exist in neighboring areas such as industrial parks. The unique system ID prevents the different networks from interfering with each other. The next four bytes, called Level 1, Level 2, Level 3, and Level 4, represent the hierarchy system of addressing. Level 1 addresses all clocks within a  
25       given system ID. Level 2 addresses a subset of all the clocks within a given system ID. Level 3 addresses a smaller subset, and Level 4

addresses the smallest subset of all clocks within a given system ID. The sixth byte is a unit number. The unit number identifies a particular clock within the subset identified by Level 1 through Level 4, and provides for selection of only one clock.

5        This header is always provided by the base station prior to the time, text, and audio data. When the header is received by a terminal, the microcontroller will decode the address and respond based on the highest level which is enabled. For instance, if Level 1 and Level 2 are not enabled, but Level 3 is, then only the terminals addressed in Level 3 will  
10    respond. This scheme allows a single address to activate a group of clocks, which is a very efficient way of utilizing RF bandwidth.

      The present invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. For instance, it should be understood by one skilled in the art that although the  
15    synchronous clock system was shown here with the PA functionality, it can function perfectly without such a capability. So for users who do not desire the PA feature, the components relating to the feature such as the microphone 48, amplifiers 48 and 80, speakers, etc. may be omitted. Of course, some changes in the microcontroller and the system control  
20    software should be made to reflect the change. Similarly, the message board 76 may also be omitted or replaced with some other external device without unduly affecting the present system.

      Moreover, although many of the other features shown herein are highly desired and preferred, it should be understood that some of the  
25    features may be omitted without unduly affecting the performance of the invention. For instance, although here the RTCs 36 and 64 and the

internal clock of the base station PC are utilized as safeguards, it is possible to operate the current system without such clocks by relying solely on the reference time source. Or in the alternative, only one or two such clocks mentioned can be used instead of using all three. Furthermore, 5 although here the reference time signal was taken from a TV broadcast, any other reliable and extractable time reference source can be used. In addition, the type of modulation scheme employed herein or the frequency used for the transmission is not the only possible choice.

The presently disclosed embodiments are, therefore, to be 10 considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are, therefore, to be embraced therein.

**CLAIMS**

This Sheet Has Been Replaced



I Claim:

| REPLACED SHEETS                              |                              | SG |
|----------------------------------------------|------------------------------|----|
| <input type="checkbox"/> Description         | : paged ..... to paged ..... |    |
| <input checked="" type="checkbox"/> Claim(s) | : paged ..12 to paged ..16   |    |
| <input type="checkbox"/> Drawing(s)          | : paged ..... to paged ..... |    |
| <input checked="" type="checkbox"/> Abstract | : paged ..... to paged ..17  |    |

- 1 1. A wireless synchronous clock system comprising:
  - 2 a base station having
    - 3 a means for obtaining a reference time signal,
    - 4 a means for modulating said time signal to a form which can
    - 5 be wirelessly transmitted,
    - 6 a means for wirelessly transmitting said time signal which has
    - 7 been modulated, and
    - 8 a first processor means for processing said time signal;
  - 9 at least one clock terminal separated from said base station, said
  - 10 terminal having
    - 11 a means for receiving said transmitted signal;
    - 12 a means for demodulating said signal received by the
    - 13 receiving means;
    - 14 a means for displaying time from said demodulated signal;
    - 15 a second processor means for processing said signal;
  - 16 whereby time displayed on said time displaying means is synchronized
  - 17 with time corresponding to said reference time signal.
- 1 2. The wireless synchronous clock system as recited in claim 1 further
  - 2 comprising a watchdog each of said first and second processor means
  - 3 for resetting said processor means when it hangs.
- 1 3. The wireless synchronous clock system as recited in claim 2 further
  - 2 comprising a user input device.



\* C L M S \*



- 1 4. The wireless synchronous clock system as recited in claim 1  
2 wherein said modulating means is a FFSK modulator.
- 1 5. The wireless synchronous clock system as recited in claim 4  
2 wherein said demodulating means is a FFSK demodulator.
- 1 6. The wireless synchronous clock system as recited in claim 1  
2 wherein said time signal is modulated and transmitted at RF frequency.
- 1 7. The wireless synchronous clock system as recited in claim 1  
2 wherein said means for obtaining a reference signal includes a  
3 VHF/UHF antenna and a time extractor.
- 1 8. The wireless synchronous clock system as recited in claim 1  
2 wherein said means for wirelessly transmitting said time signal is an  
3 antenna and a transmitter.
- 1 9. The wireless synchronous clock system as recited in claim 1 further  
2 comprising a public address system, said public address system  
3 comprising:  
4 a microphone and an amplifier connected to said first processor,  
5 said microphone and an amplifier delivering audio signal to said  
6 transmitter means;  
7 a speaker and amplifier connected to said second processor means,  
8 said speaker and amplifier receiving audio signal from said receiver  
9 means and broadcasting said audio signal through said speaker; and  
10 a means for discriminating between audio and time signals.
- 1 10. The wireless synchronous clock system as recited in claim 3 further  
2 comprising a message display board connected to said second  
3 processor means for displaying text messages, and a means for  
4 discriminating between text, and time signals.





1 11. A wireless synchronous clock system comprising:  
 2 a base station having a base station PC, a baseband  
 3 processor, a VHF/UHF antenna, and an RF antenna;  
 4 said base station PC including a time extractor and a system  
 5 software, said time extractor extracting time information from a signal  
 6 received via said VHF/UHF antenna and generating a reference time  
 7 signal, and said system software controlling system processes;  
 8 said baseband processor including a microcontroller for  
 9 receiving and processing said reference time signal, a FFSK modulator  
 10 for modulating said reference time signal, an RF transmitter for  
 11 transmitting said reference time signal modulated on an RF frequency;  
 12 at least one clock terminal separated from said base station,  
 13 said terminal having an RF receiver for receiving said time signal  
 14 transmitted by said RF transmitter, a FFSK demodulator for  
 15 demodulating said time signal, a microcontroller for controlling terminal  
 16 processes, a display for displaying time from said time signal, and a  
 17 display driver for controlling said display;  
 18 whereby time displayed on said time displaying means is  
 19 synchronized with time corresponding to said reference time signal.

1 12. The wireless synchronous clock system as recited in claim 11 further  
 2 comprising a real time clock providing a time signal to said terminal,  
 3 said real time clock being updated by said reference time signal.

1 13. The wireless synchronous clock system as recited in claim 11 further  
 2 comprising a real time clock providing a time signal to said baseband  
 3 processor when a said baseband processor is disconnected with said  
 4 base station PC.





- 1 14. The wireless synchronous clock system as recited in claim 12  
2 wherein said reference time signal is first used to update an internal  
3 clock of said base station PC.
- 1 15. The wireless synchronous clock system as recited in claim 13  
2 wherein said reference time signal is first used to update an internal  
3 clock of said base station PC.
- 1 16. The wireless synchronous clock system as recited in claim 11 further  
2 comprising a watchdog which resets said microcontroller in said  
3 baseband processor when said microcontroller hangs.
- 1 17. The wireless synchronous clock system as recited in claim 11 further  
2 comprising a watchdog which resets said microcontroller in said  
3 terminal when said microcontroller hangs.
- 1 18. The wireless synchronous clock system as recited in claim 11 further  
2 comprising a public address system, said public address system  
3 comprising:  
4 a microphone and an amplifier connected to said microcontroller in  
5 said baseband processor, said microphone and an amplifier delivering  
6 audio signal to said transmitter means;  
7 a speaker and amplifier connected to said microcontroller in said  
8 terminal, said speaker and amplifier receiving audio signal from said  
9 receiver means and broadcasting said audio signal through said  
10 speaker; and  
11 a means for discriminating between audio and time signals.
- 1 19. The wireless synchronous clock system as recited in claim 11 further  
2 comprising a user input device.





- 1 20. The wireless synchronous clock system as recited in claim 19 further  
2 comprising a message display board connected to said second  
3 processor means for displaying text messages, and a means for  
4 discriminating between time and text signals.
- 1 21. The wireless synchronous clock system as recited in claim 11  
2 wherein said terminals have a unique address, and said reference time  
3 signal contains a header for addressing the terminals.
- 1 22. In a system having a base station and a plurality of terminal clocks, a  
2 method of wirelessly synchronizing said terminal clocks comprising:  
3 obtaining a reference time signal at the base station;  
4 converting said time signal in a form which can be transmitted  
5 wirelessly;  
6 transmitting said time signal wirelessly to said terminal clocks;  
7 receiving said time signal by said terminals;  
8 converting said time signal in a form which can be displayed on a  
9 display;  
10 displaying time corresponding to said time signal.

