

WORD LINE DRIVER AND MEMORY DEVICE

ABSTRACT

The embodiments of the disclosure relate to a word line driver and a memory device. The word line driver includes a PMOS area, a NMOS area, first gates, and second gates. The PMOS area includes first active areas extending along a first direction. The first active area includes a first channel area, a first source area and a first drain area. The NMOS area includes second active areas. The second active area includes a second channel area, a second source area, a second drain area, a third channel area, a third source area, and a third drain area. The first gate, the first source area and the first drain area constitute a pull-up transistor, the first gate, the second source area and the second drain area constitute a pull-down transistor, the pull-up transistor and the pull-down transistor are electrically connected with the same sub word-line, and the extension direction of the first gate corresponding to the first active area is inclined compared with the first direction. The second gate covers the third channel area. The second gate, the third source area and the third drain area constitute a holding transistor. A third drain area of a holding transistor is electrically connected to the pull-down transistor, and a third source area of the holding transistor is electrically connected to the other pull-down transistor.

[Fig. 3]