ABSTRACT

A METHOD TO FABRICATE A ROBUST AND RELIABLE MEMORY DEVICE

A new method of forming non-volatile memory cells that prevents ion implantation induced damage in the manufacture of an integrated circuit device has been achieved. A tunneling dielectric layer is formed overlying a semiconductor substrate. A first polysilicon layer is deposited. The first polysilicon layer and the tunneling dielectric layer are patterned to form floating gates. An interpoly dielectric layer is deposited. A second polysilicon layer is deposited. The second polysilicon layer and the interpoly dielectric layer are patterned to form control gates overlying said floating gates. A masking layer is deposited overlying the control gates and the semiconductor substrate. The photoresist layer is patterned to form implantation openings in the masking layer for planned heavily doped junctions and to form isolated rings of the masking layer surrounding the implantation openings. Ions are implanted through the implantation openings to thereby complete the heavily doped junctions and the non-volatile memory cells. The isolated rings of the masking layer reduce the antenna effect and do not induce charge flow into the tunneling dielectric layer.

FIGURE 5 IS SUGGESTED FOR PUBLICATION