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ABSTRACT

Single bit nonvolatile memory cell and methods for programming and erasing thereof

5 A single bit, non-conductive floating gate memory cell
1, is introduced which can operate at ultra low voltages.
Substrate bias is used to promote the injection of carriers
into the floating gate, resulting in lower voltages to
program and erase the memory cell. The memory cell 1 is
10 arranged in an array of bit lines BL running perpendicular
to the program line PL and word lines WL. Adjacent memory
cells in each column share either a common source 3 or a
common drain 4 node. The bit line BL connects the source
nodes 3 in each column, while the program line connects the
15 drain node 4 of memory cells at corresponding positions in
each line. The reduced programming voltage allows the use
of lower program inhibit voltages on the bit line BL.

Figure 7